

Accelerated Multi-Grid Scheme for Substrate Coupling Modeling and Analysis

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Abstract— This paper proposes a novel method for substrate coupling modeling and analysis. This method is based on accelerated Multi-Grid, finite difference simulation. In this method the final value of impedance in each stage of modeling is calculated by considering the results of both two previous stage grids. This calculation performed with different weighting factors for two previous stages. This method, with best weighting factors result in 75% decrease in simulation time for low frequency substrate modeling compare with simple Multi-Grid method. The time saving will improve with increasing the accuracy and number of points for simulation.

Index Terms— Substrate coupling modeling, Multi-Grid, Finite difference method

I. INTRODUCTION

INTEGRATED CIRCUITS are popularly called systems-on-a chip (SOC), and can include both digital and analog circuits on the same chip. Size of the system is reduced in a one-chip solution, and the circuits can generally operate faster when they are on the same chip. Putting both digital and analog circuits on the same chip amplifies an important noise source affecting the analog circuitry caused by switching of the digital circuits on the chip.

The subject of substrate noise has received great attention over the recent years due to the potentially harmful consequences in large and complex system on chip, especially at high frequencies [1].

There are several mechanisms which cause substrate noise generation in digital circuits. The most significant mechanisms

are impact ionization currents and capacitive coupling from junctions [2,3,4].

Experiments show that at 0.13 micron technology, noise generation of Digital circuits on a SOC increased by 50 percent and the noise sensitivity factor of analog circuits increased 100 percent [5]. Therefore knowledge is needed on how to minimize the interference between different circuits and devices on the chip. More specifically, models are needed that can, at the circuit level, predict how much unwanted interaction there will be between different components [6].

So far, several schemes have been proposed for substrate parasitic extraction in the literature. Some researchers have used device simulators such as MEDICI, DAVINICH and PISCES to study the problem [7,8]. They have modeled the substrate distributive nature by a simple circuit of a few resistances between two devices. It is not possible to study a large circuit using this approach, because of the huge time consumption appears for accurate modeling of the substrate.

Some others have used macroscopic models such as Boundary Element Methods in recent years and used specific Green functions for solving related equations [9,10].

Among these, the numerical solution of Laplace equation on a three dimensional substrate structure, based on Finite element or Finite difference methods, (FEM and FDM) have been the most popular [7].

FDM and FEM are although attractive because of their simplicity of use and adaptability in dealing with virtually any type of substrate profile which are not practical even for medium size ICs [7]. Several efforts have been done for accelerating the Simple FDM, Among them Multi-Grid based substrate coupling model extraction shows the best performance in decreasing time for simulation [11].

In this paper a new accelerated scheme is proposed for decreasing the time of simulation in substrate coupling modelling and analysis. This scheme is based on applying weight to the results of each stage of Multi-Grid processing, and using the results of both previous stage, and before previous stage to find the new stage variables. This method, with best weighting factors results in 75% decrease in simulation time for substrate modeling compare with simple

Manuscript received May 30, 2006. This work was supported in part by University of Tehran.

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Multi-Grid method. The time saving will improve with increasing the number of points and hence increasing the accuracy of simulation.

In section II fundamentals of FDM for substrate coupling modeling and analysis is reviewed. Next the Multi-Grid method definitions are introduced and its efficiency in decreasing the time of simulation is performed. In section IV our new accelerated scheme is proposed with details, and eventually results are compared in simple FDM, simple Multi-Grid and accelerated Multi-Grid method.

II. FINITE DIFFERENCE METHOD

In FDM the substrate is discretized to a set of elementary cubic blocks as shown in Fig 1[12, 13].

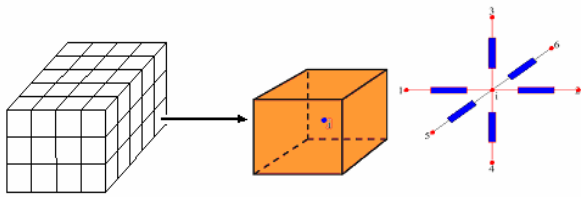


Fig. 1. Dividing substrate for FDM

The potential is assumed to be constant in each block and denoted by $\varphi_{i,j,k}$ where (i, j, k) are coordinates of the blocks. In the electrostatic case, the potential φ in the medium can be obtained by the solution of the Laplace equation subject to the given boundary conditions. The Laplace equation can be written as:

$$\frac{\partial^2 \phi}{\partial x^2} + \frac{\partial^2 \phi}{\partial y^2} + \frac{\partial^2 \phi}{\partial z^2} = 0 \quad (1)$$

Then potential at the (i,j,k) point can be obtained by [14,15].

$$\varphi_{i,j,k} = \frac{\Delta\varphi_i / R_x + \Delta\varphi_j / R_y + \Delta\varphi_k / R_z}{2/(R_x + R_y + R_z)} \quad (2)$$

As a result, each node potential can be determined by the potential of neighboring nodes. Writing Laplace equation in each node, with considering the nearest nodes presents the voltage of each node as [14, 15,16].

$$V_{i,j} = (V_{i,j-1,k} + V_{i,j+1,k} + V_{i+1,j,k} + V_{i-1,j,k} + V_{i,j,k-1} + V_{i,j,k+1})/6 \quad (3)$$

By setting out the node voltage equations for all nodes a matrix equation formed and should be solved for substrate as [10]

$$\vec{V}(n+1) = \vec{A}\vec{V}(n) + \vec{B} \quad (4)$$

Where, V is the vector of node voltages. Therefore, the substrate can be modeled as a cubic network for resistors in frequencies up to few GHZ. For upper frequencies a capacitive factor is parallelized with the resistance factor for considering the capacitive behavior of substrate in substrate coupling Analysis.

III. MULTI-GRID SCHEME

To speed up the total run time of the FDM algorithm the Multi-Grid starts its calculation with the minimum numbers of possible grid points. That is, just consider points at the boundaries condition of the region plus one point at the middle of each region. It then calculates the problem using the Gauss-Seidel algorithm until it converges. Having lost the required precision because of quite larger distance between points, Impedance vector yet contains values that are now quite closer to the real values and they even obey the same curve as that of the real values. Adding new points between each pair of previous ones as shown in Fig 2, the algorithm then exploits the calculated values to initial value of the next stage, which now has twice the elements and the distance is also divided by two. at this stage different order of Lagrange interpolation formula can be used to obtain different orders of the Multi-Grid algorithm according to the Multi-Grid algorithm according to the nature of the considered problem. This process is repeated until all the distances values of the region decrease to a value that satisfy the precision required, or it has satisfactory accuracy for results.

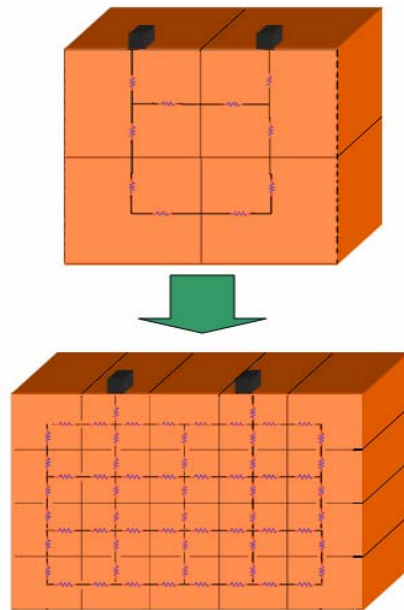


Fig. 2. First two stages of Multi-Grid processing

The role of Multi-Grid method is that it considers the final voltages of points at the previous stage as the initial values for solving ongoing matrix equation.

In third stage, the initial magnitudes for solving equation 4 are considered as the final voltages of nodes in the second stage. This process will be continued until the voltages of nodes haven't significant difference between two last stages. In that stage the potentials of nodes have been converged to a specified magnitude and the simulation is finished.

This kind of applying initial condition for solving matrix equation 4, instead of applying random magnitudes to variables, named as Multi-Grid shows a significant reduce in simulation time as shown in Fig. 3.

As shown in this figure, Multi-Grid method shows its power for simulating substrate especially with increasing the number of nodes for simulation.

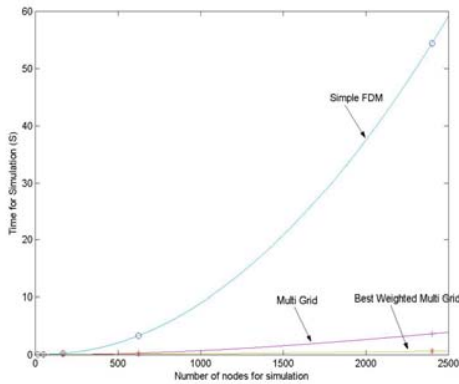


Fig. 3. Comparison of different methods for substrate coupling modeling and analysis

IV. ACCELERATED MULTI-GRID SCHEME

In the accelerated Multi-Grid method, the initial values for solving matrix equation 4 are calculated by applying both the previous stage and before previous stage results in each new stage.

For example, for calculating the initial values of variables in a $16 \times 16 \times 16$ matrix, this equation should be used:

$$I_{16 \times 16 \times 16} = w_1 I_{8 \times 8 \times 8} + w_2 I_{4 \times 4 \times 4} \quad (5)$$

In this equation $I_{16 \times 16 \times 16}$ is the initial condition by considering $16 \times 16 \times 16$ number of nodes for simulating substrate. $I_{8 \times 8 \times 8}$, and $I_{4 \times 4 \times 4}$ are the final calculated results by considering $8 \times 8 \times 8$ number of nodes, and final calculated results by considering $4 \times 4 \times 4$ number of nodes simulating for substrate.

w_1 and w_2 are the weighting factors of each stage. It also should be considered that w_1 and w_2 should have the relation below for proper approximating of the initial condition.

$$w_1 = 1 - w_2 \quad (6)$$

It should be considered that in equation 5 a $8 \times 8 \times 8$ matrix should convert to a $16 \times 16 \times 16$ matrix by defining a new point between each 2 nearest points and get its value as the average of values of nearest points.

This process should be used for converting the $4 \times 4 \times 4$ matrix, to a $8 \times 8 \times 8$ matrix, and then converting the resulted $8 \times 8 \times 8$ matrix to a $16 \times 16 \times 16$ matrix.

Different weights (w) show different times of simulation in each stage in Fig. 4.

In this figure $w = w_1$, which used in equation 6.

There are 3 separated curves or numbers of points (nodes) for simulation in this figure (169, 625, and 2401).

In 169 Points curve, it could be seen that high w have better simulation time, in compare with low w (weight). But in 2401 number of nodes for simulation, the low w have better performance of simulation time.

So, It is obvious from this figure that w should be high in the first stages of processing (around 0.8 to 0.9). This amount of w in these stages shows the more dependency of the first stages on only the previous stage, but not to the before previous stage.

The reason for this dependency is that the need for high velocity of convergence in first stages of simulation. But after passing some stages the stability of variables should be considered not to jump between two values in each stage. So lower w should be used, like weights between 0.1 and 0.2, to increase the stability of the system in late stages.

In these stages preventing from forming a loop to jump between two specified magnitudes in amount of a variable is more important, which usually occurred in overfitted models.

So the w factor should be decreased from 0.9 in early stages to 0.1 in the last stage.

By applying this kind of distribution of weights in accelerated Multi-Grid method the simulation time decrease by 75 % in 2401 number of nodes considering for simulation, compare with simple Multi-Grid method as shown in Fig. 3.

From fig. 3 it also appears that, the time saving will improve with increasing the number of points for simulation by using either simple Multi-Grid method or weighted (accelerated) Multi-Grid method compare with simple FDM. This improvement will help to simulate substrate coupling in complex system on chips which works at high frequencies.

In this kind of systems, there are several parts interfering at same time on a node to change its potential.

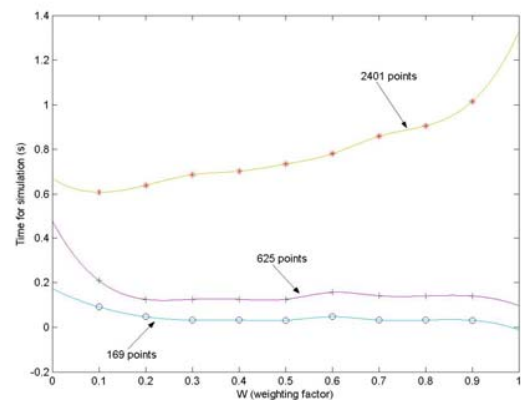


Fig.4. Simulation time for considering different number of simulation nodes and different weighting factors

V. CONCLUSIONS

In this paper a new accelerated scheme was proposed for decreasing the time of simulation in substrate coupling modelling and analysis.

This scheme was based on applying weight to the result of each stage of Multi-Grid processing, and using the results of the previous stage, and before previous stage to find the magnitudes of new stage variables. This method, with the best weighting factors, results in 75% decrease in simulation time for substrate modeling compare with simple Multi-Grid method. The accuracy of simulation for convergence was considered to be constant in both methods. The time saving

will improve with increasing the number of points for simulation and hence the increasing accuracy of simulation, by using this accelerated Multi-Grid method.

REFERENCES

- [1] R. Gharepurey and E. Charbon "Substrate coupling modeling simulation and design perspective" 5th International symposium on Quality Electronic Design IEEE 2004
- [2] J. Briaire and K. S. Krisch "Principles of substrate cross talk generation in CMOS circuits" IEEE Transactions on computer Aided Design of integrated circuits and systems VOL.19 ,No.6 , June 2000
- [3] J. Briaire and K. S. Krisch "Substrate Injection and cross talk in CMOS circuits" IEEE 1999 Proceeding of Custom integrated circuits conference
- [4] M. Badaroglu , P. Wambacq , G. Van der Plas , S. Donay , G. G. E. Gielen and H. J. De Man "Evolution of substrate noise generation mechanisms with CMOS technology scaling" Proceeding of IEEE – TCAS July 2005
- [5] A. Onabajo "Substrate Noise Analysis and Reduction in High Frequency IC Design " PhD Seminar Northwestern Polytechnic University April 30th 2005
- [6] S. Kristiansson, F. Ingvarson "A surface potential model for predicting substrate noise coupling in IC " IEEE Journal of Solid circuits_VOL.40 No.9 September 2005
- [7] N. Masoumi "Fast and efficient modeling methods for substrate coupling in VLSI circuits," PhD Thesis, VLSI Research group, University of Waterloo 2001
- [8] N. Masoumi , M. I. Elmasry, S. Safavi-Naeini " Fast and efficient parametric modeling of contact to substrate coupling ," IEEE Transactions on Computer Aided Design (TCAD) , vol.19, No.11, pp.1282-1292 , November 2000
- [9] S. Kristiansson, S. P. Kagganti, T. Ewert, F. Ingvarson, J. Olsson, and K. O. Jeppson "Substrate Resistance Modeling for Noise Coupling Analysis " Proc. IEEE International Conference on Microelectronic Test-Structures, Monterey, CA, USA, 2003
- [10] C. Xu, T. Feiz, K. Marayam "On the Numerical stability of Green's function for substrate coupling in integrated circuits" IEEE Trans on computer Aided Design of Integrated circuits and systems April 2005
- [11] J. M. S. Silva and L. M. Silveria ," Multigrid-based substrate coupling model extraction," pp.169-172 Proceeding of ISCAS 2004
- [12] J.P.Costa, M.Cuou, L.Miguel "Prerecorrected DCT techniques for modeling and simulation of substrate coupling in mixed signal ICs" *IEEE 0-7803-4455-3 1998*
- [13] M.A.Karami, N.Masoumi , "Middle surface approximation for parallel and distributed substrate coupling simulation," to be appeared in Proceeding of IEEE international conference on Mixed design 2006
- [14] S. P. Kagganti, S. Kristiansson, F. Ingvarson, and K. O. Jeppson "Resistance modeling in 1D, 2D, and 3D for substrate networks " Nordic Semiconductor Meeting, Tampere, Finland, 2003
- [15] R.Gharepurey "Modeling and analysis of substrate coupling in integrated circuits" PhD thesis University of California at Berkeley June 1995
- [16] R.Gharepurey and G.Meyer "Modeling and analysis of substrate coupling in integrated circuits" IEEE journal of Solid-State circuits, VOL. 31, NO. 3, March 1996