Double-edge Triggered Level Converter Flip-Flop with Feedback

Azam-Sadat Seyedi and Ali Afzali-Kusha
Nanoelectronics Center of Excellence, School of Electrical and Computer Engineering, University of Tehran, Tehran, Iran,
a.seyedi@ece.ut.ac.ir, afzali@ut.ac.ir

ABSTRACT

In this paper, a double-edge triggered level converter flip-flop (DE-LCFFF) is proposed. The flip-flop makes use of the conditional discharging technique which effectively suppress the dynamic power consumption during transition time and the self-precharging technique to automatically precharge its dynamic node after enough time. An explicit double-edge pulse generator is used to further decrease the power consumption in the proposed LCFF. In addition, the use of pass gate transistors and more simplified structure in the main block of DE_LCFFF leads to a less leakage power consumption. The increase in the speed is achieved by reducing the number of the stack transistors in the discharge path and using less complicated circuit structure. When compared to the previous level converter flip-flops, the proposed LCFF shows considerable reductions in the power consumption, the delay, and the area.

1. INTRODUCTION

The power consumption of systems is critically important in modern VLSI circuits especially for low power applications. To reduce the power, the power optimization techniques should be employed at different design levels. At the circuit level, the use of low power logic cells is a very efficient method of reducing the power. The power consumption may be reduced by lowering the supply voltage (V_{DD}). The delay, however, increases as the supply voltage reduces. In Clustered Voltage Scaling (CVS) scheme, the gates (blocks) which are not in the critical path are assigned with a low supply voltage (V_{DDL}) while high V_{DD} (V_{DDH}) are applied to the gates (blocks) on the critical path [1]. If a gate with V_{DDL} drives a gate with V_{DDH}, the static power of the driven gate increases which is not acceptable. To overcome this problem, level converters should be utilized at the interface of the two types of the gates (blocks). To reduce the overhead of the level conversion, low V_{DD} clusters are followed by pipeline flip-flops which are merged with the level converters [1]. These flip-flops, which simultaneously perform latching and level shifting, are called Level Converter Flip-Flops (LCFF). Reducing the power consumed by LCFF will have a considerable impact on the total power consumption.

Several LCFFs have been proposed in the literature [1], [2], and [3]. For these flip-flops, the main attention has been in improving the performance of the circuits. Clock-Level Shifted Sense Amplifier (CSSA) flip-flop proposed in [1] is shown in Figure 1. The clock signal is level-shifted up to V_{DDH} and applied to the PMOS precharge transistors. Data is applied to the NMOS transistors and therefore doesn't need to be level-shifted. The main problem with this scheme is that the use of the level shifter for level converting the clock signal to V_{DDH}, can be very energy consuming, especially when the clock signal has a very low voltage swing [3]. Another LCFF which is called Self-Precharging Flip-Flop (SPFF) is shown in Figure 2 [2]. In this circuit, the conditional capturing and the self-precharging techniques are employed to improve the performance. However, two inverters which are used to enable the self-precharging technique cause additional delay and power consumption. In addition, the large number of transistors and the long stack paths of this circuit degrade the performance and increase the area.

In [3], the conditional discharge Double-Edge triggered Level Conversion Flip-Flop (DE-LCFF) which is shown in Figure 3 is proposed. It uses double-edge triggering technique and the conditional discharging technique to reduce the clock power consumption. In this circuit, there is a PMOS transistor which is always ON causing additional short circuit power consumption especially in high switching activities. Other problems of the circuit are its large number of transistors as well as path transistors contentions.

In this paper, we propose a pulsed LCFF which makes use of smaller number of transistors less delay and power consumption. The paper is organized as follows. Section 2 introduces the proposed level converter flip-flop. Section 3 discusses about the subthreshold leakage of LCFFs. Section 4 shows the simulation results. Finally we conclude in section 5.

2. PROPOSED LEVEL CONVERTER FLIP-FLOP

The circuit diagram of the proposed double-edge triggered level converter flip-flop with feedback (DE-LCFFF) is shown in Figure 4(a). In this flip-flop, we make use of self-precharging, conditional discharging, double-edge triggered clock pulse generator, and simpler structure to improve the performance of this flip-flop compared to its predecessors. Figure 4(b) shows an explicit dual-pulse generator used in the proposed LCFF where the pulse is generated externally, denoted as ep-LCFF. In implicit-pulse generator Level Converter Flip-Flop (ip-LCFF), the pulse is generated inside the LCFF. The explicit pulse generator has some advantages over ip-LCFF counterparts. First, for ep-LCFF, the pulse generator can be shared by neighboring LCFFs.
This sharing can help in distributing the power overhead of the pulse generator among several LCFFs. Second, deploying double-edge triggering is more straightforward in ep-LCFF than ip-LCFF [4]. Third, since the height of the NMOS path transistors in ep-LCFF is less than that in ip-LCFF, a higher speed may be expected. Consequently, ep-LCFF topology is more suited for low power and high performance applications. The pulse generator used in DE-LCFFF is very similar to the one in described in [5] and is suitable for double-edge sampling. Two signals CKb and CKnot are generated from Clock. When Clock changed to High, CKb remains Low for a period equal to the delay of two inverters while CKnot in that time remains High. In this state, MP8 and MN8 are OFF while MP9 and MN9 are ON passing Clock to Puls making it High. After CKb changes its state to High, CKnot becomes Low and, hence MP9 and MN9 turn off while MN8 turns on. Thus Puls is pulled down, the narrow pulse required for the operation of LCFF is generated by MN8. Similarly, the falling edge of the Clock

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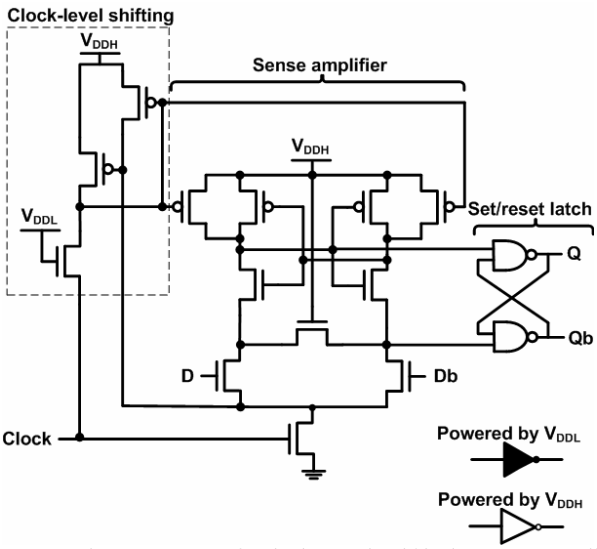

Figure 1. The structure of Clock-Level Shifted Sense Amplifier (CSSA) flip-flop [1].

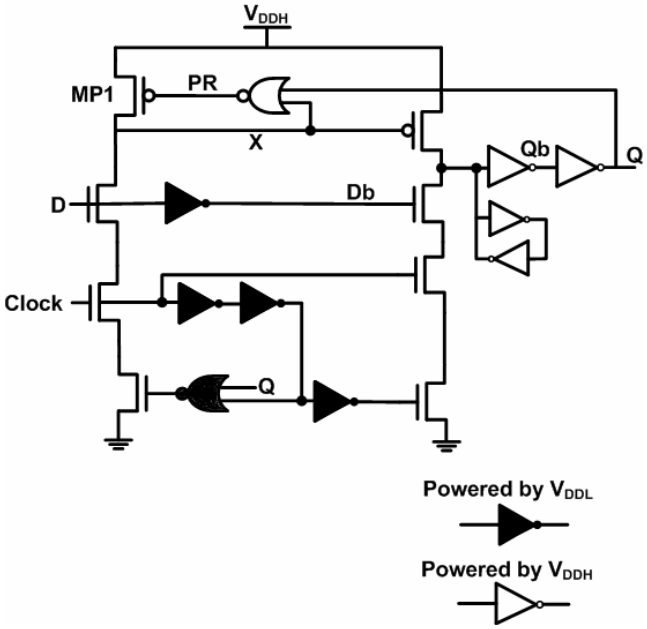

Figure 2.The structure of Self-Precharging Flip-Flop (SPFF) [2].

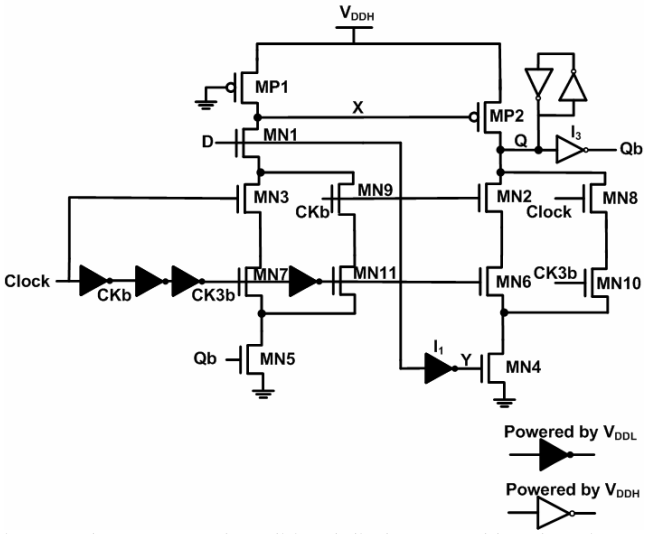

Figure 3.The structure of conditional discharge Double-Edge triggered Level Conversion Flip-Flop (DE-LCFF) [3].

leads to the generation of another pulse. As Clock goes Low, MP8 turn on taking Puls to high until CKb and CKnot go to Low and High, respectively. MP8 is turned off and MN9 and MP9 turn on. This makes Puls Low and completes the narrow pulse generation at the falling edge of the Clock.

In conventional flip-flops, due to the transitions on the clock signal, some internal nodes are precharged and evaluated in each clock cycle without producing any useful activities at the output node when the input is stable. Reducing these redundant switching activities has a profound effect in reducing the power dissipation. The conditional discharging technique has been proposed to reduce this redundant power consumption [4]. We employ the technique in our flip-flop as explained here. A discharge control signal Qb connected to MN3 is used for this purpose. When D is Low, Q is Low and Qb is High. In this case, MN3 turns on enabling the discharge path. If the input D makes a Low-to-High transition, and Puls is High, MN1 turns on, the internal node X is discharged to Low, and Q (Qb) is pulled up (down) to High (Low). This turns off MN3. For this transition of D (Low-to-High), X is discharged only once, i.e., consecutive High level at D will not be sampled because

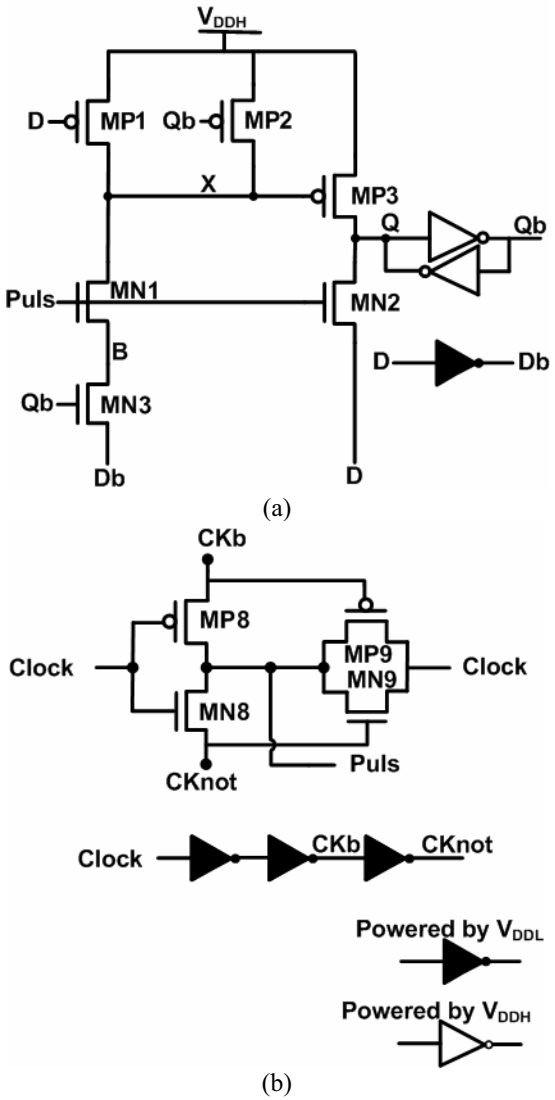

Figure 4. (a) The structure of Double-edge triggered Level Converter Flip-Flop with Feedback (DE-LCFFF). (b) The proposed clock pulse generator.

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the discharging path is not enabled. Note that the prevention of redundant switchings, also leads to less switching noise generation, which is an important issue in the mixed signal circuits.

In addition, the node X remains High (precharged) in most cases, which helps simplifying the keeper structure and, hence, reducing the capacitive loading on the node X. The self-precharging is performed using a feedback pulse (Qb) and a feedforward pulse (D) connected to the gates of MP2 and MP1, respectively. In the steady state, one of the two transistors MP1 and MP2 keep node X charged or pre-charged.

Now, we describe the operation principles of the circuit. This LCFF is made up of two stages. The first stage one is responsible for capturing the Low-to-High transition. Assume D is Low so Q is Low and Qb is High, respectively. The precharging of the node X is performed by transistor MP1. If D has a transition of Low to High and Puls is High in the sampling path, MP1 turns off, Db goes Low, MN1 turns on (MN3 turned on previously) and the internal node X is discharged. As a result, the output node will be charged to High through MP3. After a delay of one inverter, Qb goes Low and MP2 turns on and MN3 turns off. In this case, the dynamic node is precharged through the transistor MP2 which is ON and the discharging path is disabled by MN3 which is off. The second stage captures the High-to-Low input transition. If D makes a transition from High to Low, the discharge path in the second stage will be enabled, allowing the output node to discharge and to correctly capture the input data. Before the transition, MP2 keeps X charged. Now, MP2 turns off, MP1 turns on and the precharging is done through MP1.

4. SUBTHRESHOLD LEAKAGE

The subthreshold or weak inversion conduction current between the source and the drain in a MOS transistor occurs when the gate voltage is below the threshold voltage (V_{th}) [6], [7]. It can be expressed as

$$I_{ds} = \mu_0 C_{ox} \frac{W}{L}(m-1)(V_T)^2 \exp[\frac{(V_g - V_{th})}{mV_T}] \times (1-\exp[\frac{-V_{DS}}{V_T}]) \quad (1)$$

where $V_T = KT/q$ is the thermal voltage, C_{ox} is the gate oxide capacitance, μ_0 is the zero bias mobility, and m is the subthreshold swing coefficient (also called body effect coefficient). This coefficient is given by

$$m = 1 + \frac{3t_{ox}}{W_{dm}} \quad (2)$$

where W_{dm} is the maximum depletion layer width and t_{ox} is the gate oxide thickness [6]. As it is obvious from (1), if $V_{DS} \approx 0$, then the subthreshold current will be approximately zero. Based on this feature, we present a brief discussion on the leakage behaviors of the previous LCFFs structures. In the CSSA structure, the large number of transistors lead to more leakage power consumption. As will be seen later, it has the highest leakage power consumption among the LCFFs discussed in this paper. In the case of DE-LCFF (Figure 3), when the node X is High, a voltage approximately equal to V_{DD} is applied across the first branch in the pull-down network which consists of MN1, two clocked transistors (MN3 and MN7 or MN9 and MN11) and MN5. On the other hand, when the node X is Low, then Q will be High and a voltage drop of approximately equal to V_{DD} exists across the output pull-down tree leading to a high voltage drop across the transistors. This again causes a large leakage current and power consumption. The situation is even worse in the case of SPFF where this voltage exists across three transistors compared to the case of DE-LCFF where four transistors exist in the pull-down network.

For the FD-LCFF circuit, the subthreshold current should be very low due to the fact that the V_{DS} of each transistor in the pull-down network will be approximately zero. Assuming D (Db) is Low (High) and the node X is High, the voltage drop across the first branch in the pull-down network will be approximately zero. When D as well as Q are High, the V_{DS} of MN2 in the output pull-down tree is approximately zero too. Therefore, the subthreshold leakage current of the LCFF is expected to be considerably lower compared to the other LCFFs.

4. SIMULATION RESULTS

All LCFFs were designed and optimized in 70 nm CMOS technology [8]. The optimizations were performed for V_{DDH} = 1V, V_{DDL} = 0.8V, T = 25°C, the output load capacitance of 50fF, the switching activity of 50%, and the clock frequency of 200MHz (100MHz) for single-edge (double-edge) triggered LCFFs. For DE-LCFFF, the explicit pulse generator was shared among a group of four LCFFs. The power of the pulse generator was therefore divided by four and added to the power of a single LCFF to obtain the total power consumption. For non-critical transistors minimum sizes were used and critical transistors were optimized to minimize the power delay product of LCFFs. Table I presents the comparison between the CSSA, SPFF, DE-LCFF and DE-LCFFF. It includes the total number of transistors, the number of clocked transistors, and the delay from the data to the output (50% to 50% propagation delay), the total power consumption (for the input data of '0' and '1' every other clock), the PDP, and the normalized PDP with respect to that of CSSA. As observed from the figures, DE-LCFFF has the minimum PDP (at least 58.06%. improvement) among all LCFFs discussed here. In terms of the power and the delay, the improvements are at least 23.71% and 43.65%, respectively. Also, note that DE-LCFFF has a lower number of transistors, which is an important feature for the applications where minimizing the area is important. The subthreshold leakage power consumptions for different LCFFs are presented in Table

Table 1. Comparison among various structures of LCFFs.

LCFF	# of Tr.	# of Clked Tr.	D-Q(ps)	Power(uW)	PDP(aJ)	PDP(Ratio)
CSSA	23	2	125.2	1.92	240.8	1
SPFF	32	4	94.2	1.16	105.0	0.43
DE_LCFF	29	4	78.8	0.97	76.6	0.31
DE_LCFFF	12+(10/4)	(6/4)	44.4	0.74	33.0	0.13

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II. Again DE-LCFFF has the least leakage power dissipation among all the LCFFs.

5. SUMMARY AND CONCLUSION

A double-edge triggered level converter flip-flop named Double-edge triggered Level Converter Flip-Flop with Feedback was proposed in this paper. Employing conditional discharging, self-precharging, explicit pulse generator, and simpler structure considerably improved the speed. In addition, the dynamic and static power consumptions as well as the area were noticeably reduced compared to the other LCFFs discussed here. The simulations were performed in a 70nm technology revealed more than 58.06%, 23.71%, and 43.65%, improvements in the PDP, the power, and the delay, respectively. In terms of the static power, the reduction was more than 58.97%.

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Table II. The leakage power of different LCFFs.

LCFF	CSSA	SPFF	DE_LCFF	DE_LCFFF
Leakage power(nW)	120.1	65.21	64.13	49.27

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