Adaptive Neural Network Model for SOI-MOSFET I-V Characteristic Including Self-Heating Effect

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Abstract—**In this paper, a model for SOI MOSFETs which considers the self-heating effect is proposed. The model which is based on a Multi Layer Perceptron (MLP) neural network, generates the drain current as a function of the gate-source voltage, drain-source voltage, and the device temperature. Based on the current, the temperature of the device channel is calculated. The neural network adapts itself with the channel temperature which can be calculated by an equivalent thermal model for the SOI device.**

Index Terms— **Silicon on insulator, Self-heating, Neural networks.**

I. Introduction

INTEGRATED CIRCUITS are currently available with transistors whose smallest lateral feature size is less than 100nm and the thinnest materials are below 2nm [1]. Such miniaturization has led to having a hundred million transistors assembled together on a chip area no larger than a few square centimeters. The integration levels are projected to reach the gigascale as the smallest lateral device feature size approaches 10 nm. The power densities, the heat generation, and the chip temperature are reaching levels that will prevent the reliable operation of integrated circuits [1]. Silicon On Insulator (SOI) technology have some advantages such as latch up immunity, higher transconductance, and reduced parasitic source and drain capacitance compared to bulk technology [2]. Despite of these benefits, some disadvantages like the kink effect and self-heating in SOI structures induced by the buried oxide (BOX) are serious problems that exist in the SOI technology [3].

The active thin-film region of SOI devices exists on a silicon dioxide insulator which is used to separate the channel from the substrate. Since the silicon dioxide insulator is also a thermal insulator, the power consumed in the active device region increase the channel temperature easily [4]. As a result of this lattice temperature increase in the thin film, a phenomena called self-heating effect occurs.

Self-heating substantially enhances the temperature and the temperature gradients in the SOI devices and integrated circuits (IC's) and result in evident degradation of SOI performance and reliability [5]. Therefore, the channel temperature should be determined exactly at any time for calculating the drain current [6,7]. This phenomena makes modeling of the I-V characteristics of SOI-MOSFET more difficult compared to the case of bulk MOSFET.

In this paper, we introduce a model for the drain current of SOI MOSFETs based on the neural network approach. The model inputs include the gate-source voltage (V_{gs}), the drain-source voltage (V_{ds}), and the device temperature (T_{∞}). This model is based on a 3-4-2-1 Multi Layer Perceptron (MLP) neural network combined with a thermal model which calculate the channel temperature (T_{ch}) based on the current and voltages of the device and their duty cycles. The model is schematically shown in Fig. 1.

The paper is organized as follows. In Section II, fundamentals of the self-heating phenomena in SOI devices are discussed while in Section III the proposed neural network model for the I-V characteristic of the SOI MOSFET is presented. The models for the channel temperature are discussed in Section IV. Finally, the summary and conclusion are given in Section V.

II. Self-heating Phenomenon in SOI Devices

At a higher drain voltage, the power consumption of the device is higher. The consumed power leads to increase in the channel temperature due to the thermal resistance of the BOX in the SOI device. The lattice temperature increase gives rise to electron mobility degradation. The self-heating of the NMOS transistor is more significant compared to the PMOS transistor due to the higher electron mobility [4]. In addition, the effect of temperature on increasing the scattering rate and hence decreasing the mobility is more for the electron [4].

As a result of this effect, the drain current decreases as the drain voltage increases. Fig. 2 shows the drain current versus the drain voltage of an SOI NMOS device with a front gate oxide of 70 Angstroms, a thin film of 800 Angstroms, and a

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buried oxide of 4000 Angstroms, a channel length of 0.2 μm, a channel width of 9.5 μm, and an operating temperature of 77 degrees of Kelvin [8].

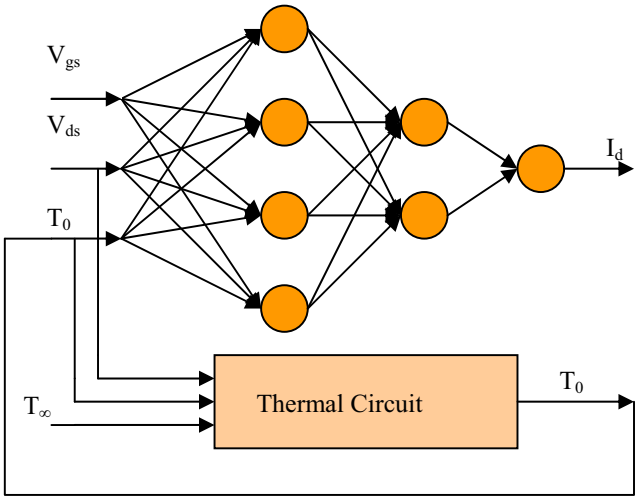

Fig. 1. Adaptive neural network system for SOI device modeling

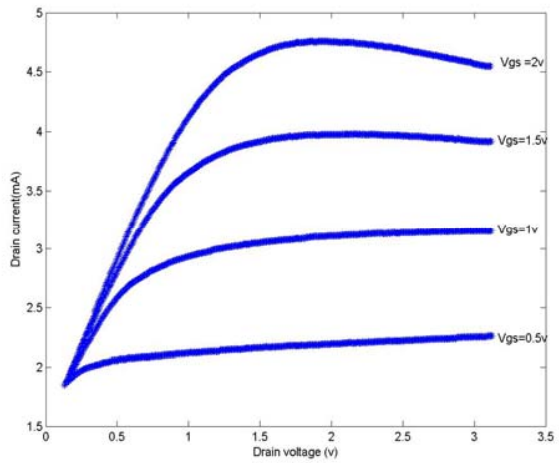

Fig. 2. The self-heating effect on the drain current [3] .

As evident from the figure, at a higher gate voltage, the self-heating effect is more noticeable.

The self-heating effect is more pronounced for SOI devices operating at low temperatures [3]. Since at low temperatures, the mobility is higher and the drain current is larger. Therefore, the power consumption and the temperature increase are higher. In addition, at low temperatures, the mobility is more sensitive to the variation in the lattice temperature [1]. Also, at low temperature, the thermal resistance of the SOI device increases due to their lower thermal conductivity [1].

III. Neural Networks Modeling of the Characteristic of SOI Devices

A computational model for the I-V characteristic SOI MOSFETs based on the neural network has been proposed in [9][10]. The modeling approach which is fast and accurate is suitable for circuit simulators. In this work, it was shown that MLPs would be better for SOI modeling compared with Radial Basis Functions (RBF) neural networks. In this paper, we add the self-heating effect to the model proposed in [9][10]. As discussed in the previous section, the temperature dependency is very important for SOI devices [11].

In this section, we use the data of the SOI device mentioned in Section II to train an 1-8-1 MLP neural network model. This neural network has one stage with eight units in that stage which generates one output. The I-V characteristic for this device obtained from the model is shown in Fig. 3.

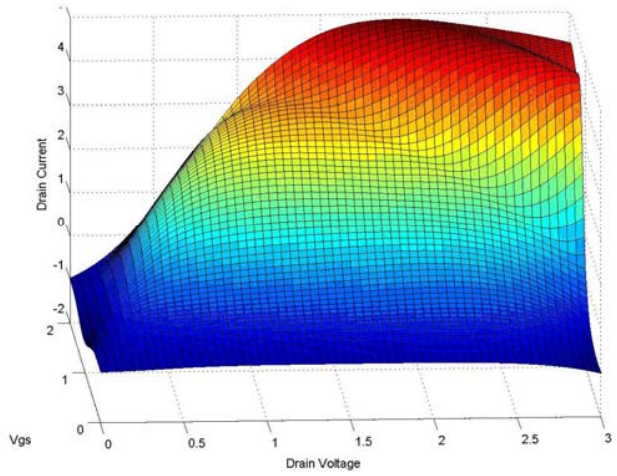

Fig. 3. Drain current (mA) versus V_{gs} and V_{ds} of SOI obtained from the MLP neural network model.

The I-V characteristic of a SOI NMOS transistor with a front gate oxide of 175 Angstroms, a thin film of 800 Angstroms, and a buried oxide of 3800 Angstroms, obtained from another neural network model is shown in Fig. 4. The neural network model for this device is a 3-4-2-1 MLP neural network which has the temperature as an additional input. The model is shown in Fig. 1. The activation functions of this neural network are "tansig" type which has two stages with four and two units in each stage, respectively. This neural network is the model proposed in this work for considering the self-heating effect. It has the channel temperature as an additional input with respect to the inputs of the neural network of [9][10]. The network was trained using the data obtained from the NMOS transistor at 77 and 300 degrees of Kelvin [12][13]. The figure shows the dependency of the drain current on the drain voltage and the channel temperature. In this figure, the model shows that, the drain current of SOI device decrease the channel temperature increases.

This model shows an error in the order of 10^{-7} for the non-trained points. This error could be reduced by increasing the stages and the units of neural network. Increasing the number of stages and units increase the complexity of the model which leads to a computation time increase. Therefore, a

trade-off between the accuracy and the complexity should be considered.

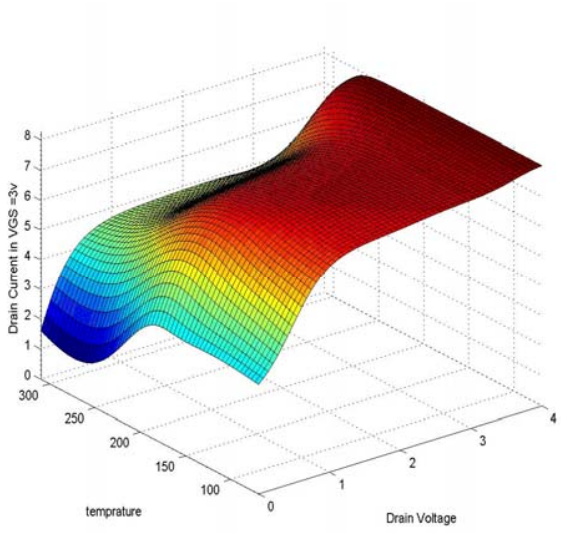

Fig. 4. Self-heating dependency of drain current.

IV. Channel Temperature Model

As discussed in the previous section, the proposed model needs the channel temperature as the input of the model. Therefore, we need to have an auxiliary model which calculates the channel temperature for the neural network model (see Fig. 1). There are two proposed different methods for calculating the channel temperature. The first simple model proposed in [14] calculates the difference in the channel temperature using

$$\Delta T = [I_{ch}.V_{ds} + I_{ch}^2(R_s + R_d)].R_T \qquad (1)$$

where R_s and R_d are the source and the drain resistors, and R_T is the thermal resistance. This resistance may be calculated from [15]

$$R_T = \frac{1}{2W}\sqrt{\frac{t_{box}}{K_{ox}K_d t_{si}}} \qquad (2)$$

where W is the device width, t_{box} is the buried oxide width, K_d is the silicon thermal conductivity, K_{ox} is the gate oxide thermal conductivity, and t_{si} is the thickness of the gate oxide. This model is simple and may not be accurate enough.

A more accurate model for calculating the channel temperature also has been introduced [1][4][7]. In this model, the channel temperature is calculated by solving the thermal circuit shown in Fig. 6. The thermal circuit has been resulted considering the thermal resistors depicted in Fig. 5. In this figure, R_{box} is the thermal resistance of the buried oxide layer, R_{ch} is the equivalent channel thermal resistance, R_{ex} is the thermal resistance of the source and the drain extensions, R_{sd} is the drain and source thermal resistances, and R_{gd} is the gate-drain thermal resistance. The thermal resistances may be calculated using [7]

$$R_{thermal} = \frac{L}{kA} \qquad (3)$$

where k is the thermal conductivity, L is the dimension along the heat conduction direction, and A is the cross-sectional area . In this equivalent thermal circuit R_g is the gate thermal resistance. R_{cd} and R_{cs} are the drain-side and source-side thermal resistances of the thin body channel. R_{xd} and R_{xs} contain R_{sd} from Fig. 5. in series with the drain-side and the source-side component of the thin channel extension, respectively. Other thermal resistances are defined in Fig. 5.

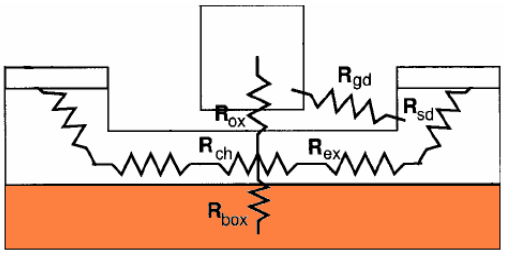

Fig. 5. Thermal resistance model of SOI [7].

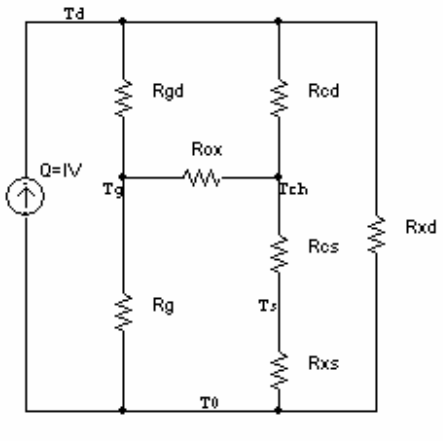

Fig. 6. Thermal circuit of SOI devices [7].

V. Summary and Conclusion

In this paper, a neural network I-V model which includes the self-heating effect for the SOI MOSFET is proposed. This model is based on a MLP neural network, which calculates the drain current of transistor by having the gate-source voltage, drain-source voltage, and the device temperature. Based on the current and voltages of the device and their duty cycle, the channel temperature is calculated using an auxiliary model. The proposed model which was a 3-4-2-1 MLP neural network had an error in the order of 10^{-7}.

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