King Fahd University of Petroleum & Minerals

College of Computer Sciences and Engineering

Department of Computer Engineering

COE 202: Fundamentals of Computer Engineering (071)

Assignment 3

(Note: All references to the text book are made to M. Morris Mano, "Digital Logic and Computer Design", Prentice-Hall, 1979.)

1. Design BCD to 7 segment display using ROM.

2. Design a circuit that changes the binary code to gray code using DCD/Encoder.

3. Design a combinational circuit that detects an error in the representation of a decimal digit in BCD. In other words, obtain a logic diagram whose output is logic-1 when the inputs contain an unused combination in the code.

4. Implement the four Boolean functions listed using three half-adder circuits (Fig. 4-2e on page 120 of the text book).
   a. D = A xor B xor C
   b. E = A'BC + AB'C
   c. F = ABC' + (A" + B')C
   d. G = ABC

5. Implement the Boolean function:
   F = AB'CD' + A'BCD' + AB'C'D + A'BC'D
   with exclusive-OR and AND gates.

6. Implement an 8x1 Multiplexer.

7. Design an excess-3-to-BCD code converter using a 4-bit full-adders MSI circuit

8. (a) Using the AND-OR-INVERT implementation procedure, (described in Section 3-7 on page 93 of the text book), show that the output carry in a full-adder circuit can be expressed as:

   $$C_{i+1} = G_i + P_i C_i = (G_i P_i + G_i C_i)'$$

   (b) IC type 74182 is a look-ahead carry generator MSI circuit that generates the carries with AND-OR-INVERT gates. The MSI circuit assumes that the input terminals have the compliments of the G's, the P's, and of C_1. Derive the Boolean functions for the look-ahead carries C_2, C_3, and C_4 in this IC. (Hint: Use the equation-substitution method to derive the carries in terms of C'_i).

9. How many don't-care inputs are there in a BCD adder?

10. Modify the BCD-to-decimal decoder of Fig. 5-10 (page 170 of the text book) to give an output of all 0's when any invalid input combination occurs.

11. Design a BCD-to-excess-3 code converter with a BCD-to-decimal decoder and four OR gates.
12. A combinational circuit is defined by the following three functions:
    a. $F_1 = x'y' + xyz'$
    b. $F_2 = x' + y$
    c. $F_3 = xy + x'y'$

    Design the circuit with a decoder and external gates.

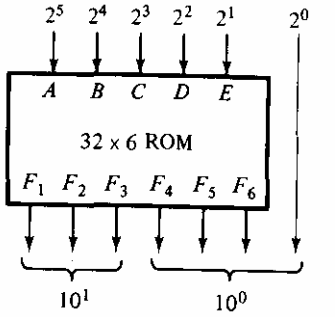
13. A combinational circuit is defined by the following two functions:
    a. $F_1(x,y) = \Sigma(0, 3)$
    b. $F_2(x,y) = \Sigma(1,2,3)$

    Implement the combinational circuit by means of the decoder shown in Fig. 5-12 (page 172 of the text book) and external NAND gates.

14. Construct a 5 X 32 decoder with four 3 X 8 decoder/ demultiplexers and a 2 X 4 decoder. Use a block diagram construction as in Fig. 5-14 (page 173 of the text book).

15. Implement a full-adder circuit with multiplexers.

16. The 32 X 6 ROM together with the 2^0 line as shown in the following figure converts a 6-bit binary number to its corresponding 2-digit BCD number. For example, binary 100001 converts to BCD 011 0011 (decimal 33). Specify the truth table for the ROM



17. Prove that a 32 X 8 ROM can be used to implement a circuit that generates the binary square of an input 5-bit number with $B_0 = A_0$ and $B_1 = 0$ as in Fig. 5-24(a)

(page 187 of the text book). Draw a block diagram of the circuit and list the first four and the last four entries of the ROM truth table.

18. Derive the PLA program table for a combinational circuit that squares a 3-bit number. Minimize the number of product terms. (See Fig. 5-24 (page 187 of the text book) for the equivalent ROM implementation.)

19. List the PLA program table for the BCD-to-excess-3 code converter defined in Section 4-5 on page 125 of the text book.