King Abdullah University of Science and Technology

Computer Science Program

CS 282 Syllabus – Spring 2010
Computer Architecture and Organization

Professor: Muhamed Mudawar
Office: Building 1, room 4210
Office Hours: Tuesday 10:30 am – 12:30 pm
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Catalog Description

Prerequisite: CS 209. Advanced topics in cache hierarchies, memory systems, storage and IO systems, interconnection networks and message-passing multiprocessor systems (clusters). Issues such as locality, coarse-grain parallelism, synchronization, overlapping communication with computation, hardware/software interfaces, performance/power trade-offs and reliability. Characteristics of modern processors that affect system architecture. Credits: (3-0-3)

Textbook

John Hennessy and David Patterson, *Computer Architecture: A Quantitative Approach*, Fourth Edition, Morgan Kaufmann Publishers, 2007, ISBN: 0-12-370490-1

Prerequisites by Topic

Basic background in: computer organization, assembly language programming, instruction pipelining, memory hierarchies, and digital design.

Grading Policy

Assignments:	20%
Research Project:	50%
Midterm Exam:	30%

Research Project

A research project will be conducted during the semester. Since there is a large class this spring semester, research will be carried by groups of four or five students. Simulation should be performed and performance results should be obtained. Your work should be reported in the form of a conference-style research paper.

Course Topics

Week	Course Topics	Reading
1, 2	**Fundamentals of Computer Design** Classes of computers, instruction set architecture, technology trends, performance trends, power in integrated circuits, cost, dependability, computer performance, CPU time, CPI, MIPS, FLOPS, Amdahl's law, Benchmarks.	Chapter 1
3, 4	**Pipelining: Basic Concepts** Classic five-stage pipeline for a RISC processor, structural hazards, data hazards and forwarding, branch hazards, performance of a pipeline with stalls, pipeline implementation, dealing with exceptions, handling multicycle operations.	Appendix A
5 - 7	**Instruction Level Parallelism and Advanced Pipelining** ILP concepts, data dependences and hazards, control dependences, loop unrolling and compiler scheduling, static and dynamic branch prediction, Tomasulo dynamic scheduling, hardware-based speculation, multiple-issue processor, VLIW approach, advanced pipelining and speculation, limits of ILP.	Chapters 2, 3
8 - 10	**Memory Hierarchy Design** Typical memory hierarchy, cache memory concepts, cache organization, cache performance, reducing cache hit, misses, and miss penalty, multi-level caches, advanced cache optimizations, memory technologies, virtual memory.	Chapter 5 Appendix C
11 - 13	**Multiprocessors and Thread-Level Parallelism** Classification of parallel architectures, models for communication and memory architecture, symmetric shared memory, cache coherence, snooping protocols, distributed shared memory, directory-based coherence, synchronization, memory consistency.	Chapter 4