COE 308 – Computer Architecture
Term 072 – Spring 2008

Computer Engineering Department
College of Computer Sciences & Engineering
King Fahd University of Petroleum & Minerals

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Catalog Description

Memory hierarchy and cache memory. Integer and floating point arithmetic. Instruction and arithmetic pipelining, superscalar architecture. Reduced Instruction Set Computers. Parallel architectures and interconnection networks.

Prerequisites: COE 205.

Textbook

David A. Patterson and John L. Hennessy, *Computer Organization and Design: The Hardware / Software Interface*, Third Edition, Morgan Kauffmann Publishers, 2005. ISBN 1-55860-604-1.

Course Objectives

- In-depth understanding of the inner-workings of modern computer systems, their evolution, and tradeoffs present at the hardware-software interface.
- Understanding the design process of a modern computer system. This includes the design of the processor datapath and control, the memory system, and I/O subsystem.

Grading Policy

Assignments and Quizzes	15%
Projects	25%
Major I Exam	20%
Major II Exam	20%
Final Exam	20%

- Written assignments should be submitted at the beginning of class time in the specified due date. Late written assignments are not accepted, especially if the solution is discussed in class.
- Late projects are accepted, but will be penalized 5% for each late day, up to a maximum of seven late days.

Software Tools used in Mini-Projects

- MARS simulator: runs MIPS-32 assembly language programs.
- LogiSim simulator: educational tool for designing and simulating CPUs.

Course Topics and Lecture Breakdown by Week

Week	Course Topics	Reading
1	Introduction to computer architecture, ISA versus organization, components, abstraction, technology improvements, chip manufacturing process.	Chapter 1
2-4	Instruction set design, RISC design principles, MIPS registers, instruction formats, arithmetic instructions, immediate operands, bit manipulation, load and store instructions, byte ordering, addressing modes, flow control instructions, pseudo-instructions, procedures and runtime stack, call and return, MIPS register conventions, alternative IA-32 architecture.	Sections 2.1 – 2.9 Sections 2.13, 2.15 – 2.18 Sections 3.2 – 3.3 Appendix A.9 – A.10
5	CPU performance and metrics, CPI, performance equation, MIPS as a metric, Amdahl's law, benchmarks and performance of recent Intel processors.	Chapter 4
6-7	Integer multiplication, integer division, floating point representation, IEEE 754 standard, normalized and de-normalized numbers, zero, infinity, NaN, FP comparison, FP addition, FP multiplication, rounding and accurate arithmetic, FP instructions in MIPS.	Sections 3.4 – 3.6 Sections 3.8 – 3.9
8-9	Designing a processor, register transfer logic, datapath components, clocking methodology, single-cycle datapath, main control signals, ALU control, single-cycle delay, multi-cycle instruction execution, CPI in a multi-cycle CPU.	Sections 5.1 – 5.5
10	Pipelining versus serial execution, MIPS 5-stage pipeline, pipelined datapath, pipelined control, pipeline performance.	Sections 6.1 – 6.3
11	Pipeline hazards, structural hazards, data hazards, stalling pipeline, forwarding, load delay, compiler scheduling, hazard detection, stall and forwarding unit, control hazards, branch delay, dynamic branch prediction, branch target and prediction buffer.	Sections 6.4 – 6.6
12-13	Cache memory design, locality of reference, memory hierarchy, DRAM and SRAM, direct-mapped, fully-associative, and set-associative caches, handling cache miss, write policy, write buffer, replacement policy, cache performance, CPI with memory stall cycles, AMAT, two-level caches and their performance, main memory organization and performance.	Sections 7.1 – 7.3 Sections 7.5 – 7.6
14	Virtual memory, address mapping, page table, handling a page fault, TLB, virtual versus physical caches, overlapped TLB and cache access.	Section 7.4