COE 308 – Spring 2006
Computer Architecture

Quiz on Multi-Cycle Processor Implementation

Wednesday, April 26, 2006

Student Name:_____ **ID:**_____

1. **(10 pts)** Describe the effect that a single stuck-at-0 or stuck-at-1 fault would have for the signals shown below, in the **multi-cycle datapath**. Which instructions, if any, will not work correctly? Explain why.

   Consider each of the following faults separately:

   a) (2 pts) RegWrite stuck-at-1
   b) (2 pts) MemRead stuck-at-0
   c) (2 pts) MemWrite stuck-at-0
   d) (2 pts) IRWrite stuck-at-0
   e) (2 pts) PCWrite stuck-at-1

2. **(10 pts)** We want to compare the performance of a **single-cycle CPU design** with a **multicycle design**. The circuit delays are as follows:

   Memory access time = 200 ps, (same for instruction fetch, data read, and data write)
   Register file access time = 150 ps, (same access time for read and write)
   ALU delay = 200 ps (same delay for all ALU instructions)

   Ignore the other delays in the multiplexers, control unit, sign-extension, etc.

   Assume the following instruction mix: 40% ALU, 20% Load, 10% Store, 20% Branch, and 10% Jump. For the multicycle design, Load instructions take 5 cycles to complete, ALU and Store instructions take 4 cycles, Branch instructions take 3 cycles, and Jumps take only 2 cycles.

   a) (3 pts) What should be the clock cycle for the single-cycle design?

   b) (2 pts) What should be the clock cycle for the multi-cycle design?

   c) (3 pts) What is the average CPI per instruction for the multi-cycle design?

   d) (2 pts) What is the speedup of multi-cycle over the single-cycle design?