COE 308 – Spring 2006
Computer Architecture

Quiz on Single-Cycle Processor Implementation

Saturday, April 15, 2006

Student Name:_____ **ID:**_____

1. **(10 pts)** Describe the effect that a single stuck-at-0 fault (i.e., the signal is always 0 regardless of what it should be) would have for the signals shown below, in the single-cycle Datapath. Which instructions, if any, will not work correctly? Explain why.

Consider each of the following faults separately:

a) RegWrite = 0
b) RegDst = 0
c) ALUScr = 0
d) MemtoReg = 0
e) Branch = 0

2. (10 pts) We want to compare the performance of a **single-cycle CPU design** with a **fixed clock cycle** to a **variable-length** clock. Suppose we add the multiply and divide instructions to the single-cycle implementation. The operation times are as follows:

Instruction memory access time = 150 ps,	Data memory access time = 200 ps
Register file read access time = 100 ps,	Register file write access = 50 ps
ALU delay for basic instructions = 150 ps,	ALU delay for multiply or divide = 400 ps

Ignore the other delays in the multiplexers, control unit, sign-extension, etc.

Assume the following instruction mix: 30% ALU, 15% multiply & divide, 25% load, 10% store, 15% branch, and 5% jump.

a) What is the total delay for each instruction class?

b) What is the average time per instruction for a variable-length clock and the speedup over a fixed-length clock cycle?