COE 308 – Fall 2005
Computer Architecture

Assignment 4: Single-Cycle Processor Implementation

Due: Saturday, November 26, 2005

1. **(5 pts)** Describe the effect that a single stuck-at-0 fault (i.e., the signal is always 0 regardless of what it should be) would have for the signals shown below, in the single-cycle Datapath. Which instructions, if any, will not work correctly? Explain why.

   Consider each of the following faults separately:

   a) RegWrite = 0
   b) RegDst = 0
   c) ALUScr = 0
   d) MemtoReg = 0
   e) Branch = 0

2. **(5 pts)** Repeat question 1 but this time consider stuck-at-1 faults (the signal is always 1).

3. **(8 pts)** We wish to add the instruction **`jalr`** (jump and link register) to the single-cycle datapath. Add any necessary datapath and control signals and draw the result datapath. Show the values of the control signals to control the execution of the **`jalr`** instruction.

   The jump and link register instruction is described below:

   ```
   jalr rd, rs  # rd = pc + 4 , pc = rs
   ```

op[6] = 0	**rs[5]**	**0**	**rd[5]**	**0**	**func[6] = 9**

4. **(2 pts)** Determine whether any of the control signals in the single-cycle implementation can be eliminated and replaced by another existing control signal, or its inverse. Consider only the following control signals: *RegDst*, *Branch*, *ALUSrc*, *MemtoReg*, *MemWrite*, and *RegWrite*. Such redundancy exists because we have used a very small set of instructions. This redundancy will disappear when we implement a larger number of instructions.