# COE 308 Syllabus – Fall 2005 Computer Architecture

Computer Engineering Department College of Computer Sciences & Engineering King Fahd University of Petroleum & Minerals

Professor:	Muhamed Mudawar, Room 22/328, Phone 4642
Office Hours:	SMW 10 – 12 noon or by appointment
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## **Catalog Description**

Memory hierarchy and cache memory. Integer and floating point arithmetic. Instruction and arithmetic pipelining, superscalar architecture. Reduced Instruction Set Computers. Parallel architectures and interconnection networks.

Prerequisites: COE 205.

#### Textbook

David A. Patterson and John L. Hennessy, *Computer Organization and Design: The Hardware / Software Interface*, Second Edition, Morgan Kauffmann Publishers, 1998. ISBN 1-55860-428-6.

## References

MIPS32 Architecture for Programmers, Volumes I, II, and III, Revision 2.50, July 2005.

## **Course Objectives**

- 1. In-depth understanding of the inner-workings of modern computer systems, their evolution, and tradeoffs present at the hardware-software interface.
  - Instruction Set Architecture
  - Performance and metrics
  - Computer Arithmetic
  - Pipelining
  - Parallelism and Multiprocessors
- 2. Understanding the design process of a modern computer system.
  - Datapath Design
  - Control Design
  - Memory System Design
  - I/O System Design

#### **Course Details**

- 1. Introduction and Performance 1 week
  - Computer Abstractions (Sections 1.1 1.3)
  - Computer Technology (Sections 1.4 1.5)
  - CPU Performance and Metrics (Sections 2.1 2.3)
  - Evaluating Performance and Benchmarks (Sections 2.4 2.6)

- 2. Instructions Set Design 1 week
  - Instruction Set Design Principles (Section 3.1 3.3)
  - Instruction Representation (Section 3.4)
  - Instruction Categories and Addressing Modes (Sections 3.5 3.8)
- 3. Computer Arithmetic 2 weeks
  - Signed and Unsigned Numbers (Sections 4.1 4.2)
  - Addition and Subtraction (Section 4.3)
  - Logical Operations (Section 4.4)
  - Constructing an Arithmetic Logic Unit (Section 4.5)
  - Multiplication and Division (Sections 4.6 4.7)
  - Floating Point representation (Section 4.8)
  - Floating Point Addition and Multiplication (Section 4.8)
  - MIPS Instruction Set (Section 4.11 and Appendix A.10)
- 4. Datapath and Control 2 weeks
  - Building a Single-Cycle Datapath (Sections 5.1 5.3)
  - Controlling the Datapath (Section 5.3)
  - Multi-Cycle Datapath and Control Implementation (Section 5.4)
- 5. Pipelined Processor Design 3 weeks
  - Pipelined Datapath (Sections 6.1 6.2)
  - Pipelined Control (Section 6.3)
  - Data Hazards and Forwarding (Section 6.4)
  - Data Hazards and Stalls (Section 6.5)
  - Branch Hazards (Section 6.6)
  - Exceptions (Section 6.7)
  - Superscalar Processors and Dynamic Pipelining (Section 6.8 6.9)
- 6. Memory System Design **3 weeks** 
  - Locality of Reference (Section 7.1)
  - Cache Memory Organization (Sections 7.2, 7.3, 7.5)
  - Read, Write, and Handling Cache Misses (Section 7.2, 7.5)
  - Cache Memory Performance (Section 7.3)
  - Virtual Memory Organization and Management (Section 7.4)
  - Real Implementations (Section 7.6)
- 7. Introduction to Multiprocessors 2 weeks
  - Multiprocessors Connected by a Bus (Sections 9.1 9.3)
  - Multiprocessors Connected by a Network (Sections 9.4, 9.5, 9.10)
  - Interconnection networks (Section 9.6)

## **Grading Policy**

Assignments and Quizzes	20%
Major Exam I	25%
Major Exam II	25%
Final Exam	30%

- Assignments should be submitted at the beginning of class time in the specified due date.
- Late written assignments are not accepted, especially if the solution is discussed in class.
- Late programming assignments are accepted, but will be penalized 10% for each late day, up to a maximum of five late days.