COE 205 Computer Organization & Assembly Language

Assignment 1 Solution

Q1. (2 pts) What is the duration of a single clock cycle (in nanoseconds) in a 3.4 GHz processor?

Solution: Clock cycle = 1 / (3.4×10^9) sec = 0.294 ns.

Q2. (2 pts) In an 8-stage non-pipelined processor, how many clock cycles would it take to execute 10 instructions?

Solution: Number of clock cycles = 8 × 10 = 80

Q3. (2 pts) In an 8-stage pipelined processor, how many clock cycles would it take to execute 5 instructions?

Solution: Number of clock cycles = 8 + 5 – 1 = 12

Q4. (2 pts) Suppose an 8-stage pipelined processor has one stage that requires two cycles to execute, how many clock cycles would it take to execute 4 instructions?

Solution: Number of clock cycles = 8 + 2×4 – 1 = 15

Q5. (2 pts) A hard disk rotates at 4200 RPM (rotations per minute). What is the time of one rotation in milliseconds?

Solution: Time of one rotation = 1 / 4200 min = 60000 / 4200 msec = 14.29 msec

Q6. (1 pt) Which Intel processor was the first member of the IA-32 family?

Solution: Intel 80386 was the first 32-bit architecture

Q7. (1 pt) Which Intel processor first introduced superscalar execution?

Solution: Intel Pentium (80586) was the first Intel superscalar processor

Q8. (2 pts) Name all 32-bit general-purpose registers

Solution: EAX, EBX, ECX, EDX, ESI, EDI, ESP, EBP

Q9. (2 pts) Name all six CPU status flags in the Intel processor

Solution: Carry (CF), Overflow (OF), Sign (SF), Zero (ZF), Parity (PF), and Auxiliary Carry (AF)

Q10. (1 pt) Which flag is set when an arithmetic or logical instruction produces a negative result?

Solution: Sign Flag (SF)

Q11. (2 pts) In real-address mode, convert the following hexadecimal segment-offset address to a 20-bit physical address: 8AF3:C91D.

Solution: 8AF30 + C91D = 9784D (hex)

Q12. (1 pt) What is the range of addressable memory in protected mode?

Solution: 4 GB, 00000000h to FFFFFFFFh