COE 205 – 02 Fall 2006
Course Learning Outcomes Evaluation Table

Outcome	Outcome Min. Weight	Assessment Method							
		Assignments	**Quizzes**	**Exam I**	**Exam II**	**Final Exam**	**Lab Work**	**Project**	**Total**
O1	**55%**	**20%**	**2%**	**15%**	**20%**			**4%**	**61%**
	Average	80.6%	78%	76.4%	76.5%			75.2%	77.8%
	Evidence	#1-6	Quiz 1	Exam I	Exam II				
O2	**4%**						**10%**		**10%**
	Average						80.7%		80.7%
	Evidence						Lab Work		
O3	**15%**		**3%**			**20%**			**23%**
	Average		62.5%			71.2%			70.1%
	Evidence		Quiz 2			Final Ex			
O4	**2%**							**4%**	**4%**
	Average							75.2%	75.2%
	Evidence								
O5	**2%**							**2%**	**2%**
	Average							75.2%	75.2%
	Evidence								
Weight		**20%**	**5%**	**15%**	**20%**	**20%**	**10%**	**10%**	**100%**
Average		80.6%	68.7%	76.4%	76.5%	71.2%	80.7%	75.2%	76.2%

COE 205 Computer Organization & Assembly Language

Course Learning Outcomes Table

Course Learning Outcomes	Outcome Indicators and Details	Assessment Methods and Metrics	ABET 2000 Criteria
1. Ability to analyze, design, implement, and test assembly language programs.	• Instruction Set Architecture • Number (unsigned and signed) and character representation • Addressing modes • Syntax, semantics, and effect on flags of Pentium instructions. • Input/output. • Arithmetic and logic operations. • Flow-control structures. • Procedures. • Macros. • String manipulation. • Interrupt mechanism. • Implementation of Pseudo code algorithms in assembly language.	• Assignments • Quizzes • Exams • Project	C(H)
2. Ability to use tools and skills in analyzing and debugging assembly language programs.	• Assembly language vs. machine language. • Assembling and linking assembly programs (including use of multiple files). • Use of debugger to analyze and debug programs. • Use of libraries.	• Lab work	K(L)

3. Ability to design the datapath and control unit of a simple CPU.	• Fetch-execute cycle • Data, address and control busses • Register transfer • Data path design: 1-bus, 2-bus and 3-bus CPU. • Derivation of control steps for assembly instructions. • Hardwired Control unit design • Microprogrammed control unit design. • Fixed vs. variable instruction format.	• Assignments • Quizzes • Exams	C(M)
4. Ability to demonstrate self-learning capability.	• Ability to learn a course topic alone (e.g. Macros) • Course Project may involve topics not studied in the course	• Assignments • Quizzes • Project	I(L)
5. Ability to work in a team.	• Project is divided into separate parts that will be integrated for project completion.	• Project	D(L)

Instructor Comments and Feedback:

Instructors need to comment here about outcomes that they think were not achieved or there is a need for improvement. The instructor needs to suggest ways for improving outcome achievement in next course offerings.

Outcome 3, which is the ability to design the datapath and control of a simple CPU, needs improvement.

Dr. Muhamed Mudawar, February 4, 2007