Analysis of Clocked Sequential Circuits

COE 202

Digital Logic Design

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Presentation Outline

- ❖ Analysis of Clocked Sequential circuits
  - ✧ State and Output Equations
  - ✧ State Table
  - ✧ State Diagram
- ❖ Mealy versus Moore Sequential Circuits
  - ✧ State and Timing Diagrams

Analysis of Clocked Sequential Circuits

Analysis is describing what a given circuit will do

The output of a clocked sequential circuit is determined by

1. Inputs
2. State of the Flip-Flops

Analysis Procedure:

1. Obtain the equations at the inputs of the Flip-Flops
2. Obtain the output equations
3. Fill the state table for all possible input and state values
4. Draw the state diagram

Analysis Example

❖ Is this a clocked sequential circuit?

YES!

❖ What type of Memory?

D Flip-Flops

❖ How many state variables?

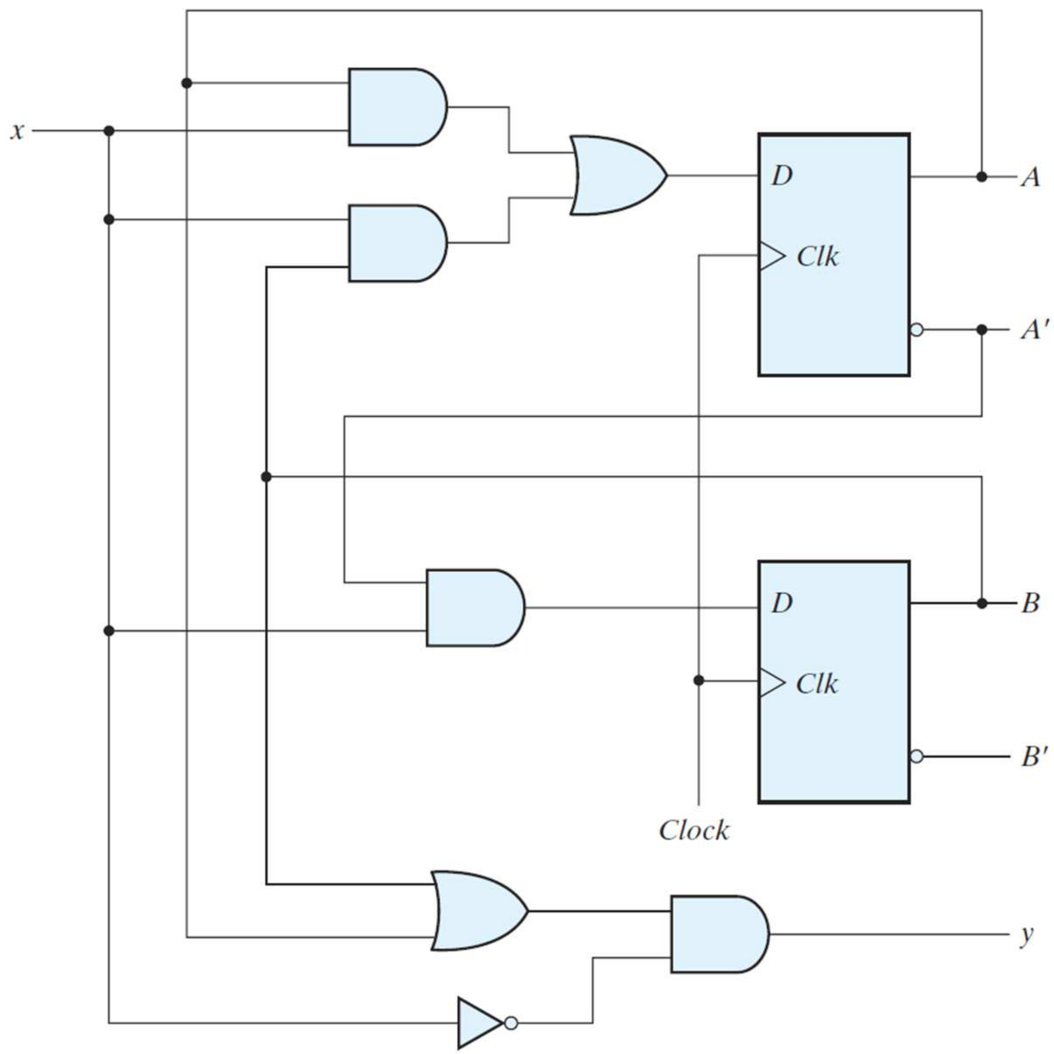
Two state variables: A and B

❖ What are the Inputs?

One Input: x

❖ What are the Outputs?

One Output: y



Flip-Flop Input Equations

- What are the equations on the D inputs of the flip-flops?

$$D_A = A\,x + B\,x$$

$$D_B = A'\,x$$

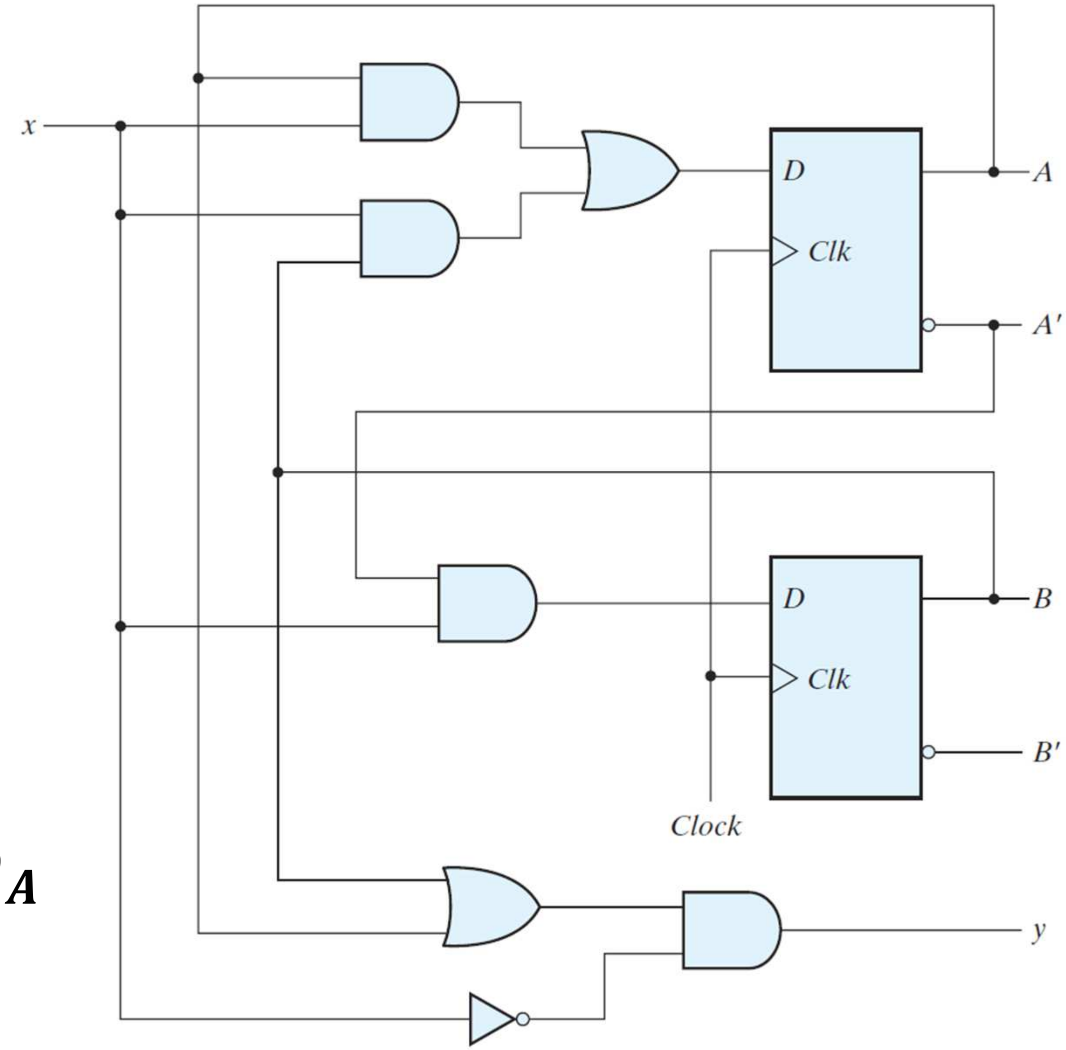
- A and B are the **current state**

$$A(t) = A,\ \ B(t) = B$$

- D_A and D_B are the **next state**

$$A(t+1) = D_A,\ \ B(t+1) = D_B$$

- The values of A and B will be D_A and D_B at the next clock edge



Next State and Output Equations

❖ The next state equations define the **next state**

At the **inputs** of the Flip-Flops

❖ Next state equations?

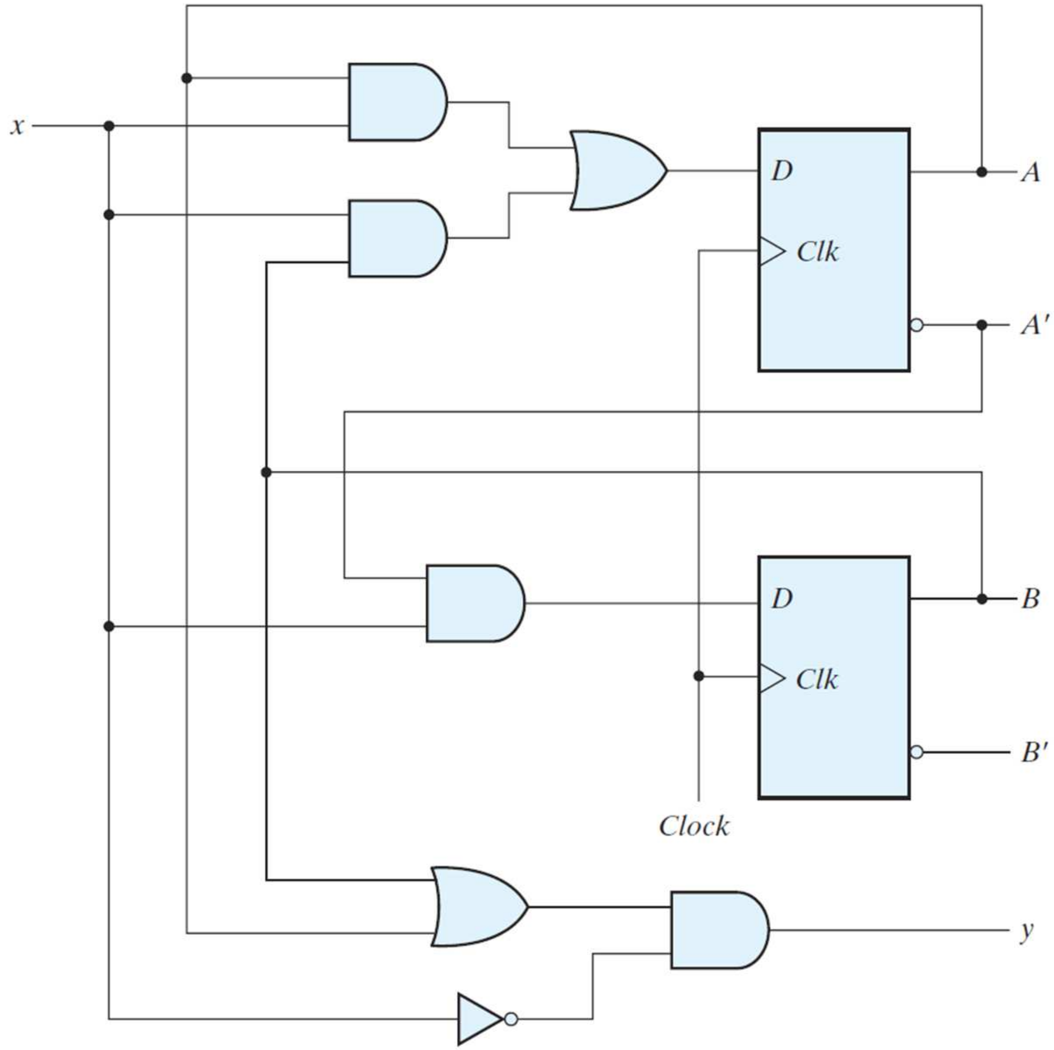
$$A(t+1) = D_A = A\,x + B\,x$$

$$B(t+1) = D_B = A'\,x$$

❖ There is only one output y

❖ What is the output equation?

$$y = (A + B)\,x'$$



State Table

❖ State table shows the Next State and Output in a tabular form

❖ Next State Equations: $A(t+1) = A\,x + B\,x$ and $B(t+1) = A'\,x$

❖ Output Equation: $y = (A+B)\,x'$

Present State A	Present State B	Input x	Next State A	Next State B	Output y
0	0	0	0	0	0
0	0	1	0	1	0
0	1	0	0	0	1
0	1	1	1	1	0
1	0	0	0	0	1
1	0	1	1	0	0
1	1	0	0	0	1
1	1	1	1	0	0

Another form of the state table

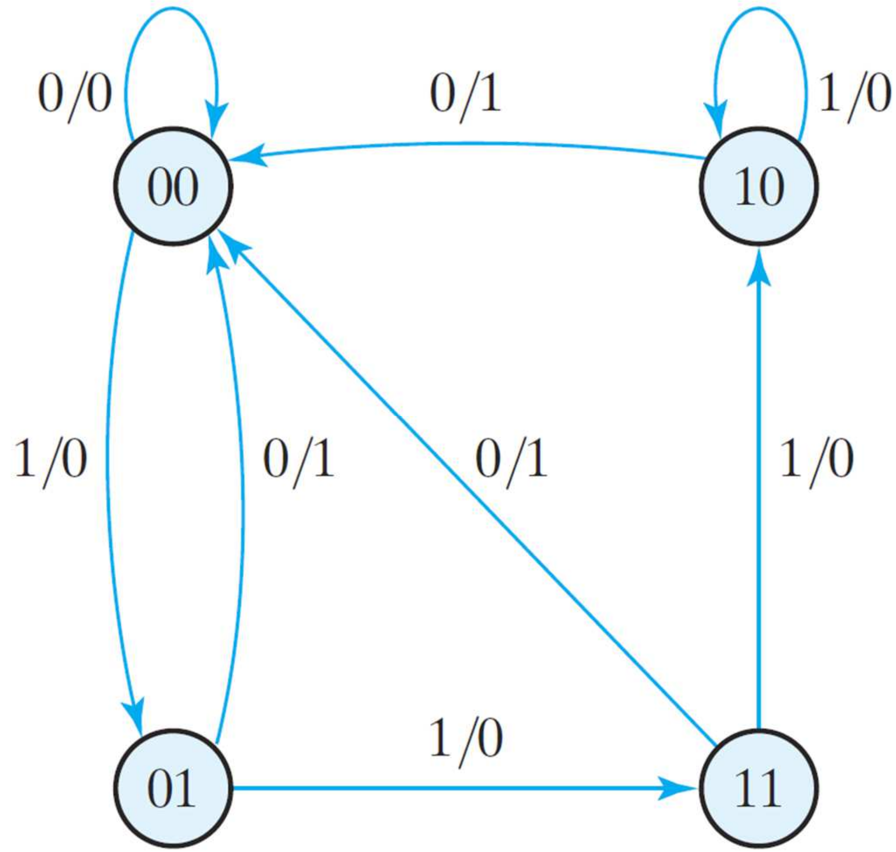
Present State		Next State				Output	
		$x = 0$		$x = 1$		$x = 0$	$x = 1$
A	B	A	B	A	B	y	y
0	0	0	0	0	1	0	0
0	1	0	0	1	1	1	0
1	0	0	0	1	0	1	0
1	1	0	0	1	0	1	0

State Diagram

- State diagram is a graphical representation of a state table
- The circles are the states
- Two state variable ➔ Four states (ALL values of A and B)
- Arcs are the state transitions

  Labeled with: Input x / Output y

Present State		Next State				Output	
		$x = 0$		$x = 1$		$x = 0$	$x = 1$
A	B	A	B	A	B	y	y
0	0	0	0	0	1	0	0
0	1	0	0	1	1	1	0
1	0	0	0	1	0	1	0
1	1	0	0	1	0	1	0



Combinational versus Sequential Analysis

Analysis of Combinational Circuits

- Obtain the Boolean Equations
- Fill the Truth Table

Output is a function of input only

Analysis of Sequential Circuits

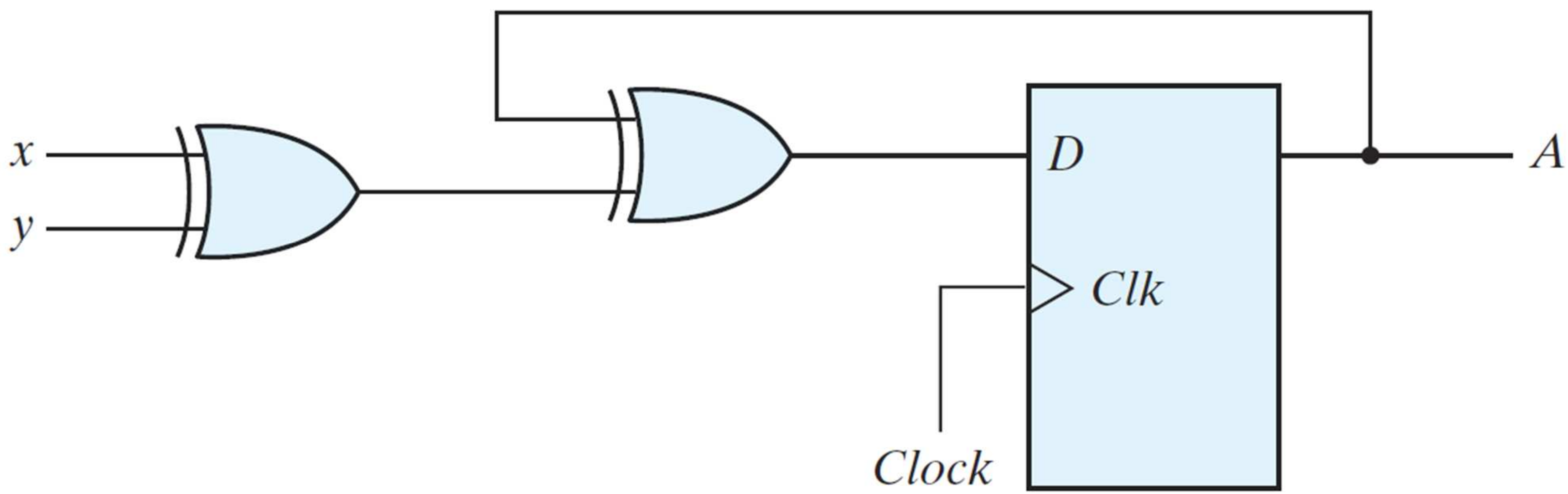
- Obtain the Next State Equations
- Obtain the Output Equations
- Fill the State Table
- Draw the State Diagram

Next state is a function of input and current state

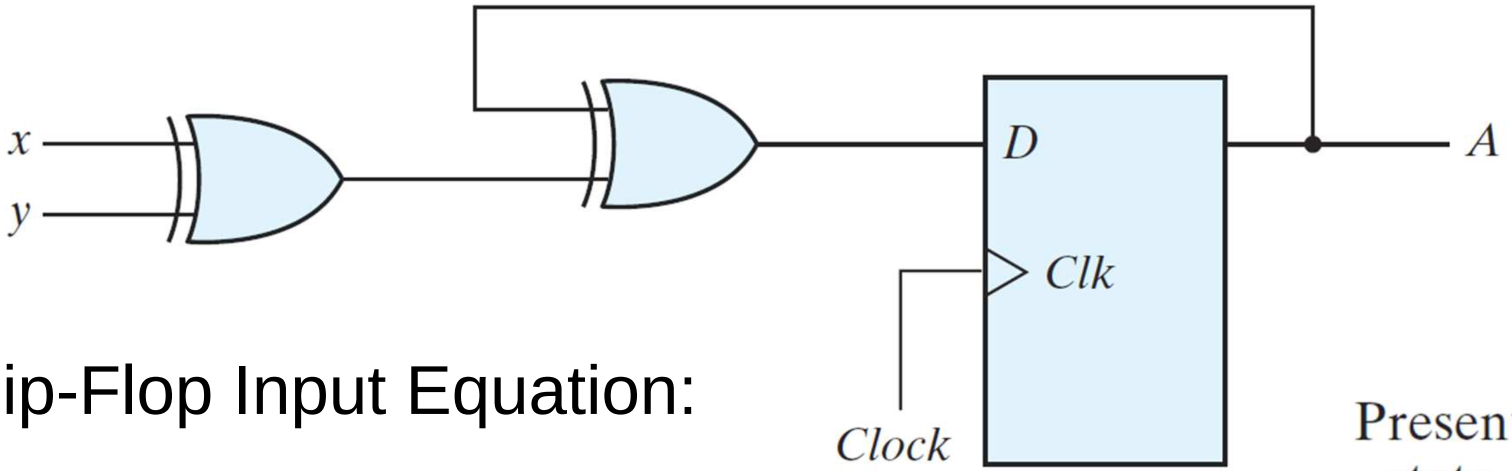
Output is a function of input and current state

Example with Output = Current State

- ❖ Analyze the sequential circuit shown below
- ❖ Two inputs: x and y
- ❖ One state variable A
- ❖ No separate output ➔ Output = current state A
- ❖ Obtain the next state equation, state table, and state diagram



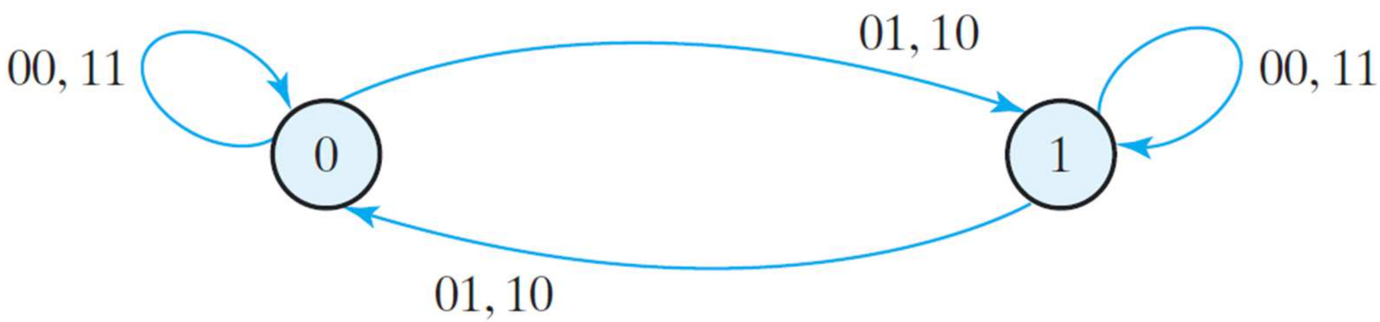
Example with Output = Current State



- Flip-Flop Input Equation:

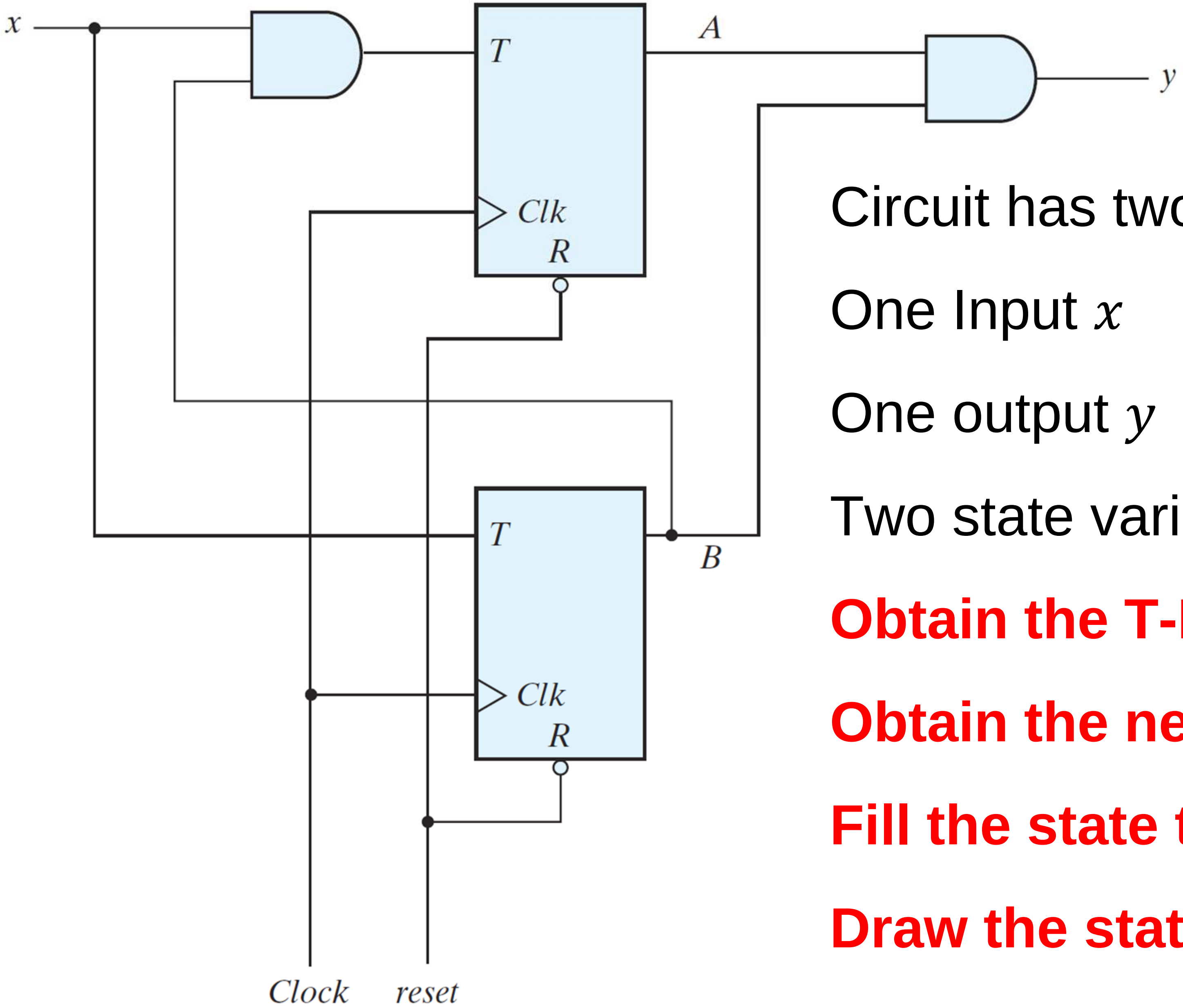
  $$D_A = A \oplus x \oplus y$$

- Next State Equation: $A(t + 1) = A \oplus x \oplus y$



Present state	Inputs		Next state
A	x	y	A
0	0	0	0
0	0	1	1
0	1	0	1
0	1	1	0
1	0	0	1
1	0	1	0
1	1	0	0
1	1	1	1

Sequential Circuit with T Flip-Flops



Circuit has two T Flip-Flops

One Input x

One output y

Two state variables: A and B

Obtain the T-FF input equations

Obtain the next state equations

Fill the state table

Draw the state diagram

Recall: Flip-Flop Characteristic Equation

- For D Flip-Flop: $Q(t+1) = D$
- For T Flip-Flop: $Q(t+1) = T \oplus Q(t)$
- For JK Flip-Flop: $Q(t+1) = J\,Q'(t) + K'\,Q(t)$

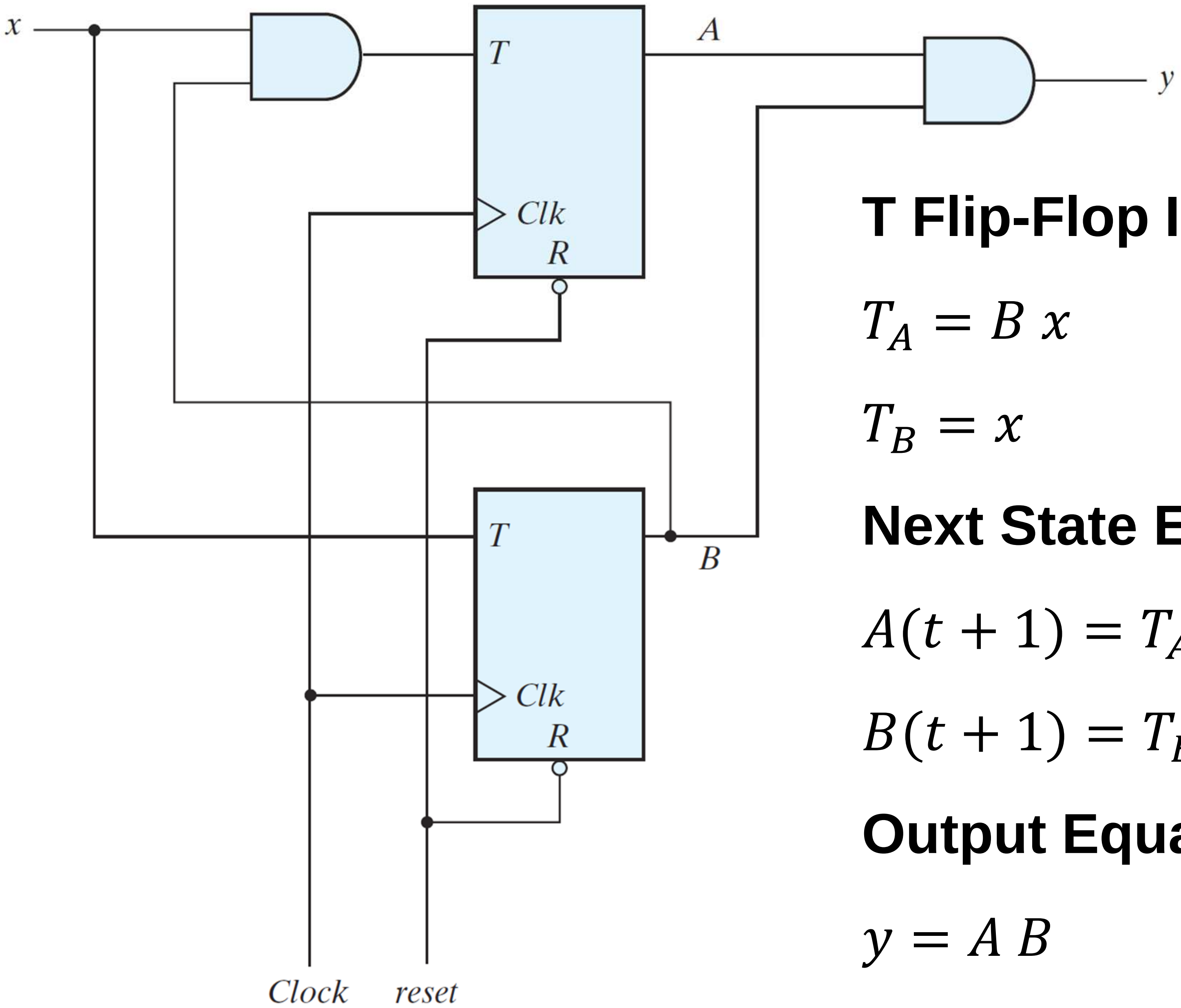
These equations define the Next State

D Flip-Flop		
D	***Q(t+1)***	
0	0	Reset
1	1	Set

T Flip-Flop		
T	***Q(t+1)***	
0	Q(t)	No change
1	Q'(t)	Complement

JK Flip-Flop		
J K	***Q(t+1)***	
0 0	Q(t)	No change
0 1	0	Reset
1 0	1	Set
1 1	Q'(t)	Complement

Sequential Circuit with T Flip-Flops



T Flip-Flop Input Equations:

$$T_A = B\,x$$

$$T_B = x$$

Next State Equations:

$$A(t+1) = T_A \oplus A = (B\,x) \oplus A$$

$$B(t+1) = T_B \oplus B = x \oplus B$$

Output Equation:

$$y = A\,B$$

From Next State Equations to State Table

T Flip-Flop Input Equations:

$$T_A = B\,x$$

$$T_B = x$$

Next State Equations:

$$A(t+1) = (B\,x) \oplus A$$

$$B(t+1) = x \oplus B$$

Output Equation:

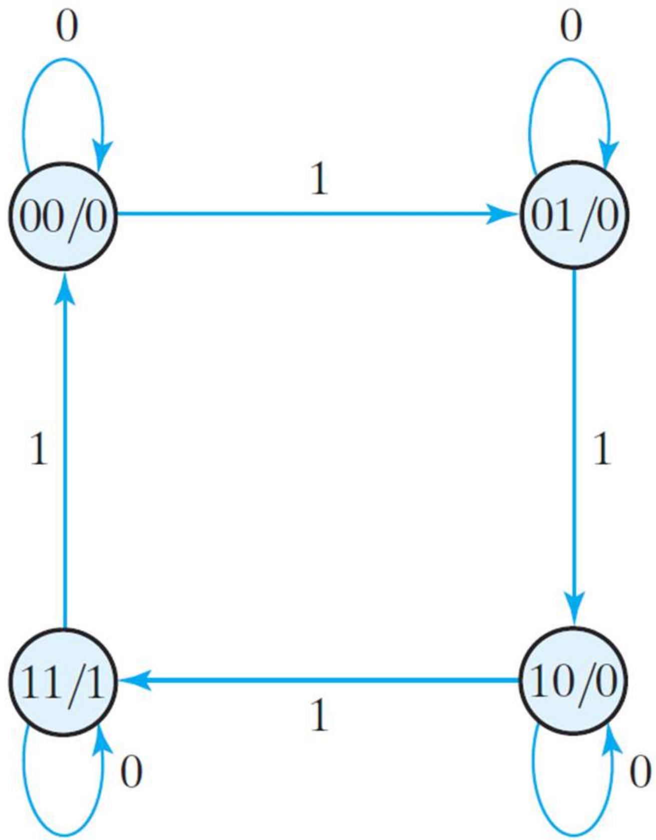
$$y = A\,B$$

Present State		Input	Next State		Output
A	*B*	*x*	*A*	*B*	*y*
0	0	0	0	0	0
0	0	1	0	1	0
0	1	0	0	1	0
0	1	1	1	0	0
1	0	0	1	0	0
1	0	1	1	1	0
1	1	0	1	1	1
1	1	1	0	0	1

Notice that the output is a function of the present state only.
It does **NOT** depend on the input x

From State Table to State Diagram

Present State		Input	Next State		Output
A	*B*	*x*	*A*	*B*	*y*
0	0	0	0	0	0
0	0	1	0	1	0
0	1	0	0	1	0
0	1	1	1	0	0
1	0	0	1	0	0
1	0	1	1	1	0
1	1	0	1	1	1
1	1	1	0	0	1



❖ Four States: $AB = 00,\ 01,\ 10,\ 11$ (drawn as circles)

❖ Output Equation: $y = A\ B$ (does not depend on input x)

❖ Output y is shown inside the state circle (AB/y)

Sequential Circuit with a JK Flip-Flops

One Input x and two state variables: A and B (outputs of Flip-Flops)

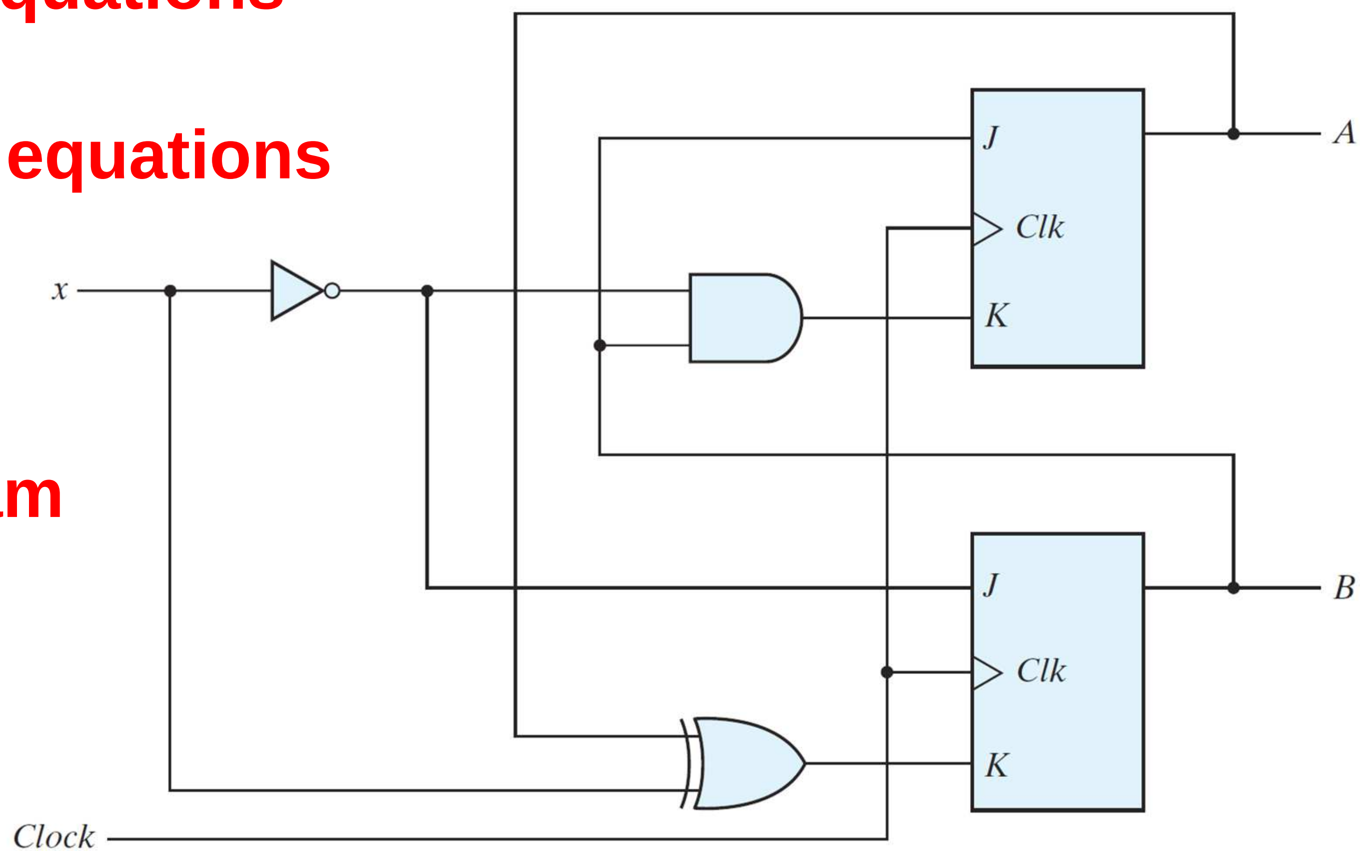
No separate output ➔ Output = Current state $A\ B$

Obtain the JK input equations

Obtain the next state equations

Fill the state table

Draw the state diagram

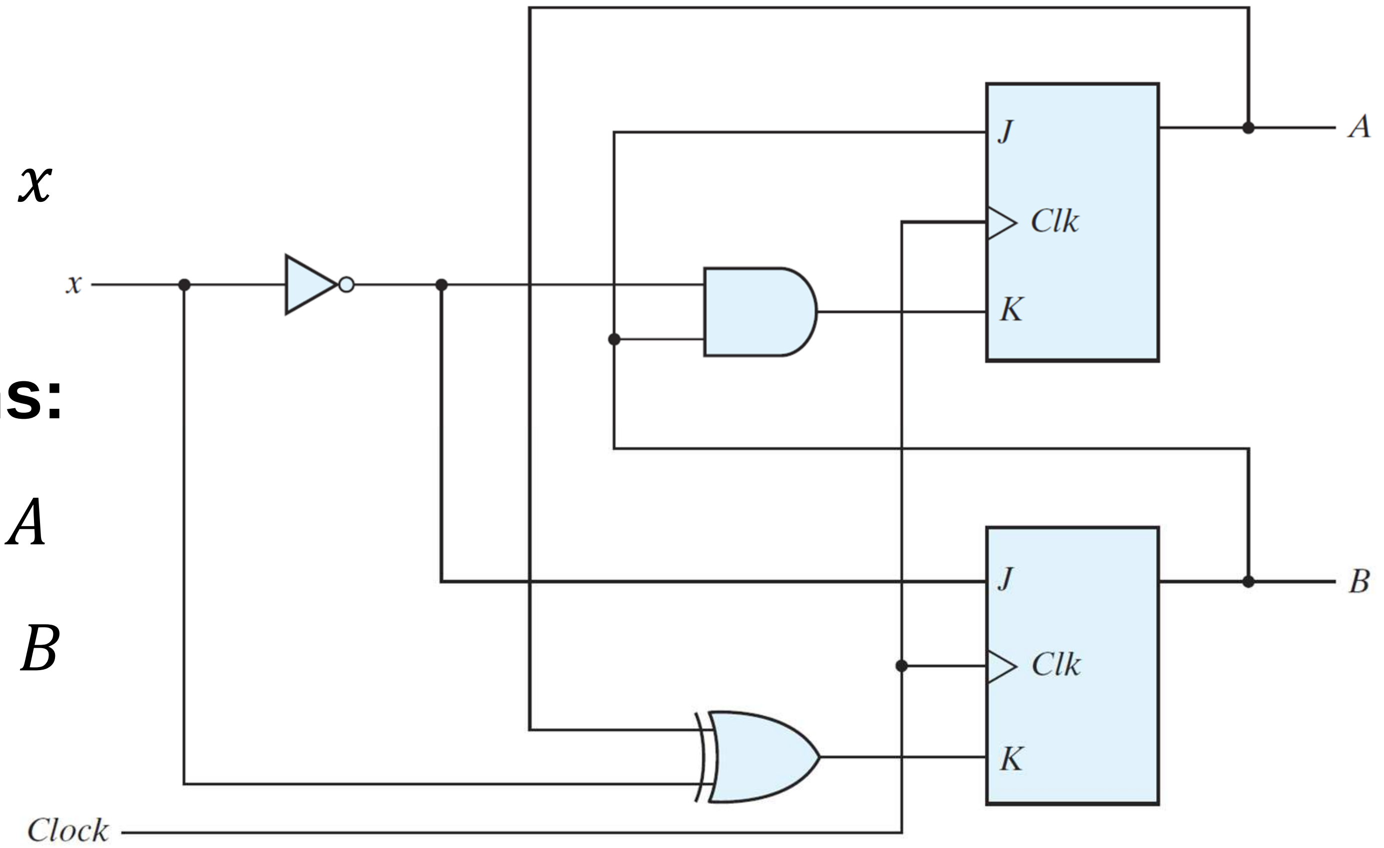


JK Input and Next State Equations

JK Flip-Flop Input Equations:

$J_A = B$ and $K_A = B\,x'$

$J_B = x'$ and $K_B = A \oplus x$



Next State Equations:

$A(t+1) = J_A\,A' + K_A'\,A$

$B(t+1) = J_B\,B' + K_B'\,B$

Substituting:

$A(t+1) = B\,A' + (Bx')'A = A'B + AB' + Ax$

$B(t+1) = x'B' + (A \oplus x)'B = B'x' + A\,B\,x + A'B\,x'$

From JK Input Equations to State Table

JK Input Equations: $J_A = B$, $K_A = B\,x'$, $J_B = x'$ and $K_B = A \oplus x$

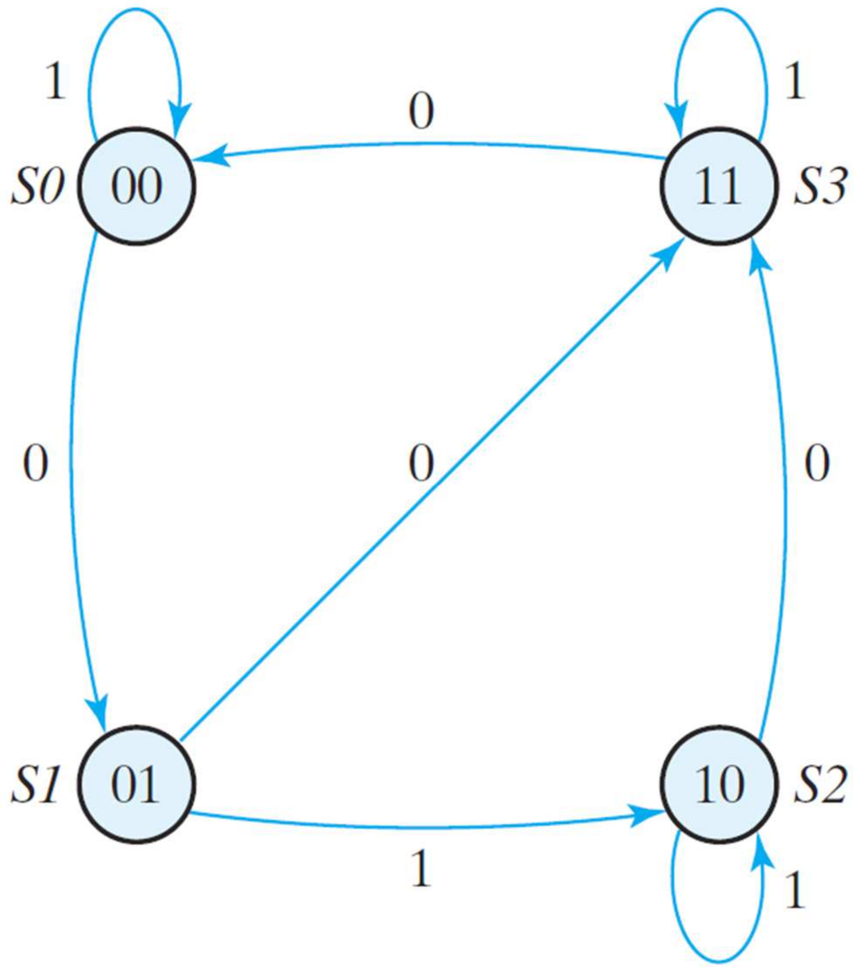
Present State		Input	Next State		Flip-Flop Inputs			
A	***B***	***x***	***A***	***B***	J_A	K_A	J_B	K_B
0	0	0	0	1	0	0	1	0
0	0	1	0	0	0	0	0	1
0	1	0	1	1	1	1	1	0
0	1	1	1	0	1	0	0	1
1	0	0	1	1	0	0	1	1
1	0	1	1	0	0	0	0	0
1	1	0	0	0	1	1	1	1
1	1	1	1	1	1	0	0	0

From State Table to State Diagram

Four states: $A\,B = 00, 01, 10, and\ 11$ (drawn as circles)

Arcs show the input value x on the state transition

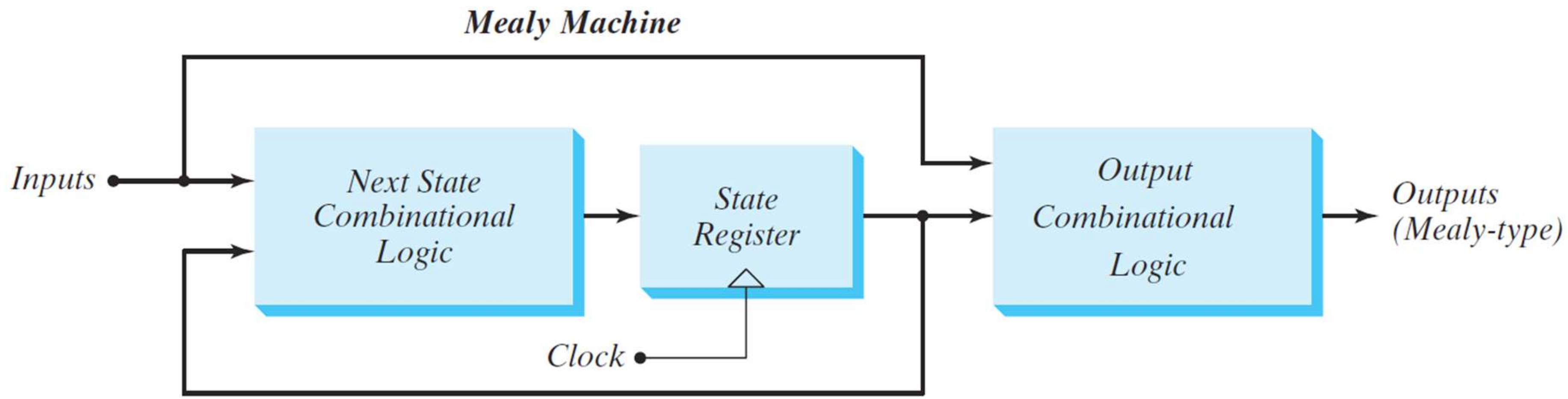
Present State		Input	Next State	
A	**B**	**x**	**A**	**B**
0	0	0	0	1
0	0	1	0	0
0	1	0	1	1
0	1	1	1	0
1	0	0	1	1
1	0	1	1	0
1	1	0	0	0
1	1	1	1	1

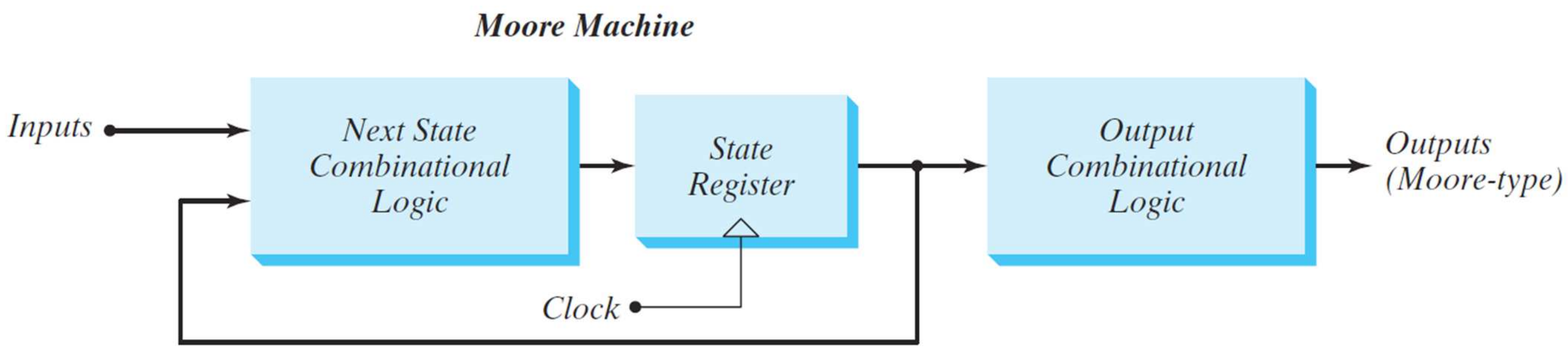


Mealy versus Moore Sequential Circuits

There are two ways to design a clocked sequential circuit:

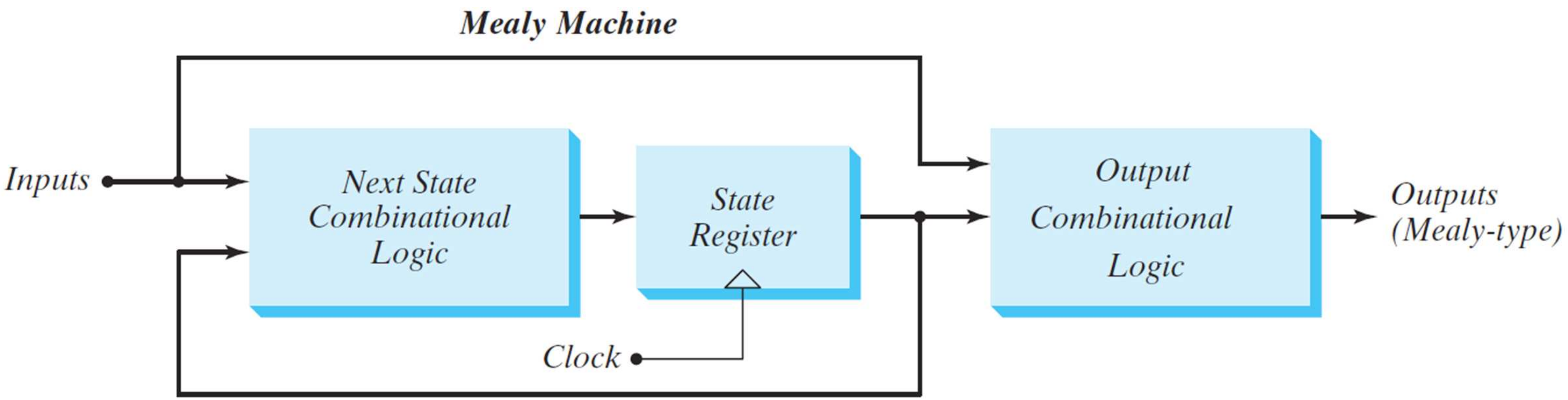
1. **Mealy Machine:** Outputs depend on present state and inputs
2. **Moore Machine:** Outputs depend on present state only





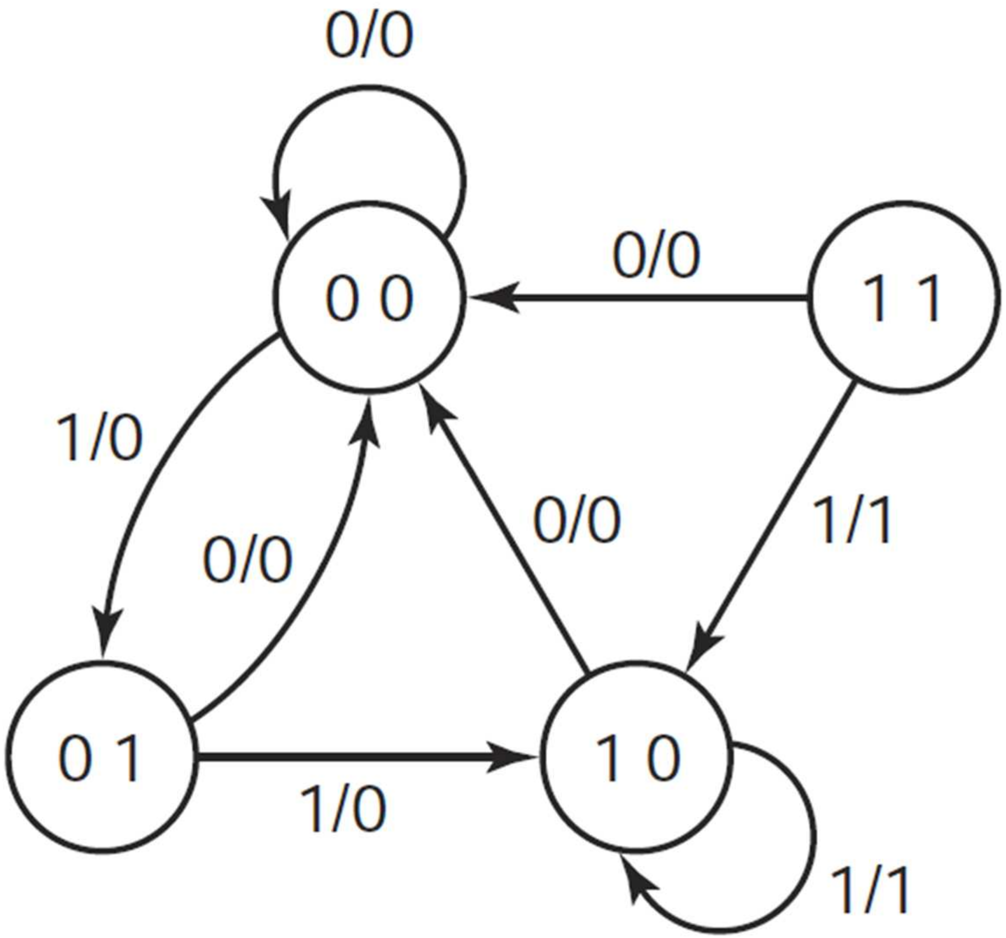
Mealy Machine

- The outputs are a function of the present state and Inputs
- The outputs are **NOT** synchronized with the clock
- The outputs may change if inputs change during the clock cycle
- The outputs may have momentary false values (called glitches)
- The correct outputs are present just before the edge of the clock



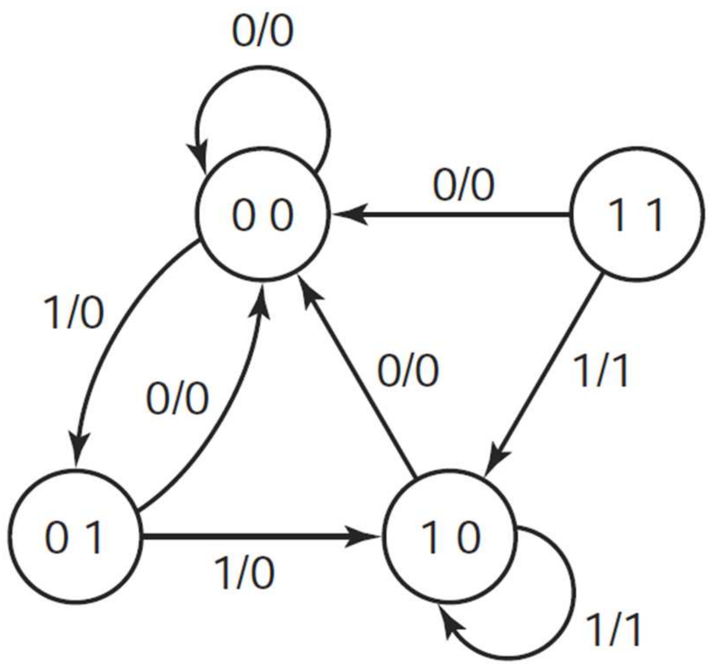
Mealy State Diagram

- An example of a Mealy state diagram is shown on the right
- Each arc is labeled with: **Input / Output**
- The output is shown on the arcs of the state diagram
- The output depends on the current state and input
- Notice that State 11 cannot be reached from the other states



Tracing a Mealy State Diagram

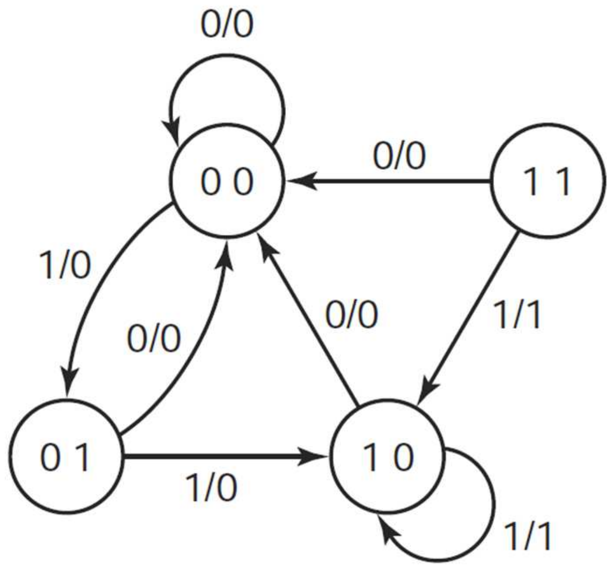
Cycle	0	1	2	3	4	5	6	7	8
Input *x*	0	1	1	0	1	1	1	1	0
Present State *A B*	?	0	0	1	0	0	1	1	1
	?	0	1	0	0	1	0	0	0
Output *z*	0	0	0	0	0	0	1	1	0

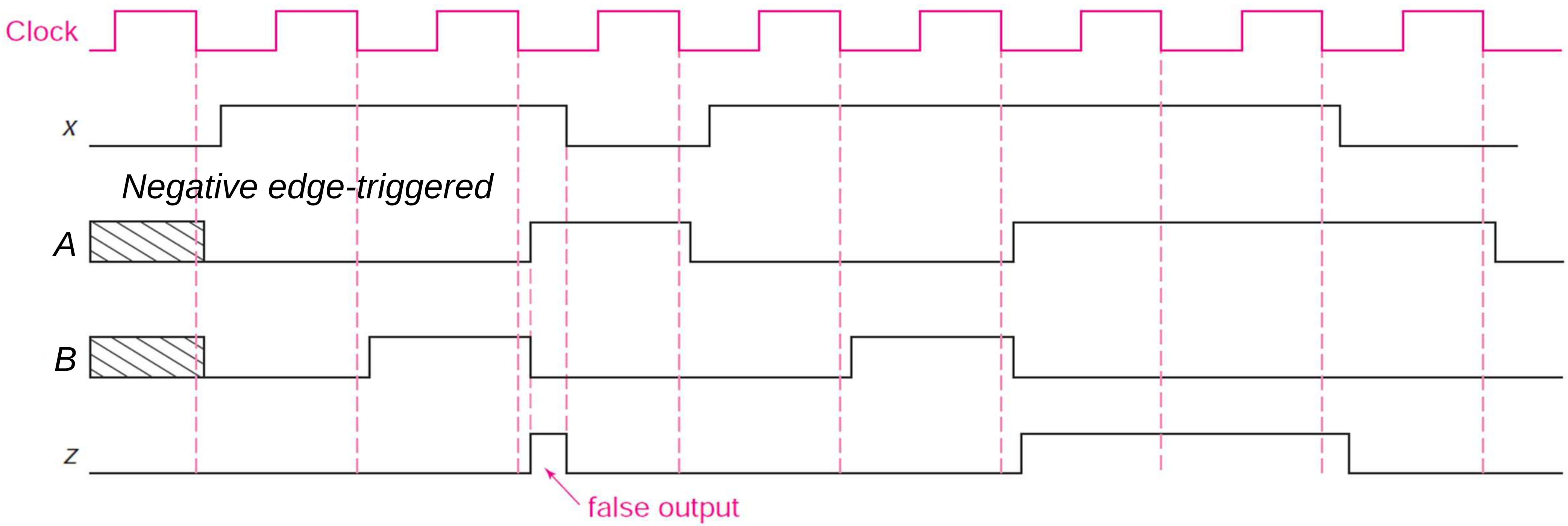


- When the circuit is powered, the initial state (*AB*) is unknown
- Even though the initial state is unknown, the input x = 0 forces a transition to state *AB* = 00, regardless of the present state
- Sometimes, a reset input is used to initialize the state to 00

False Output in the Timing Diagram

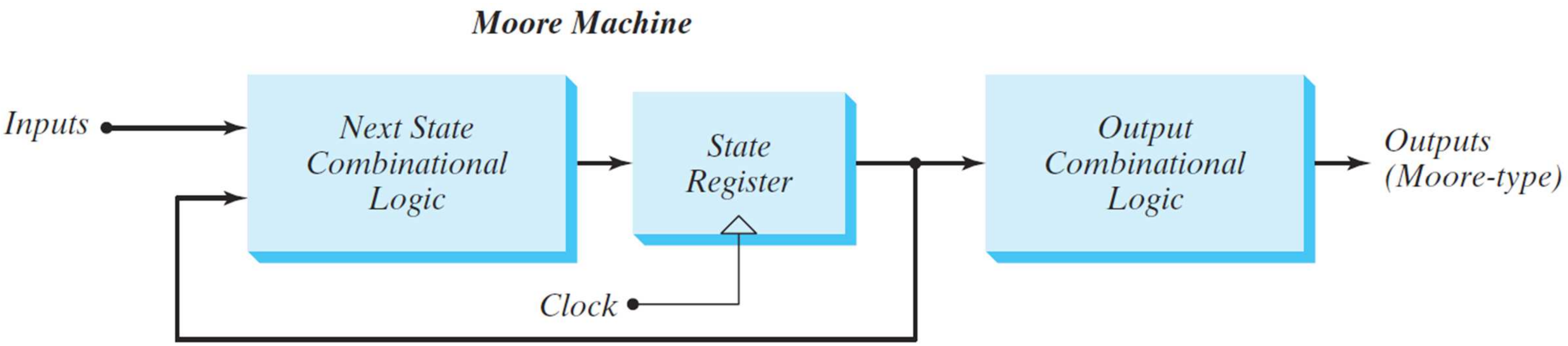
Cycle	0	1	2	3	4	5	6	7	8
Input *x*	0	1	1	0	1	1	1	1	0
Present State *A B*	?	0	0	1	0	0	1	1	1
	?	0	1	0	0	1	0	0	0
Output *z*	0	0	0	0	0	0	1	1	0





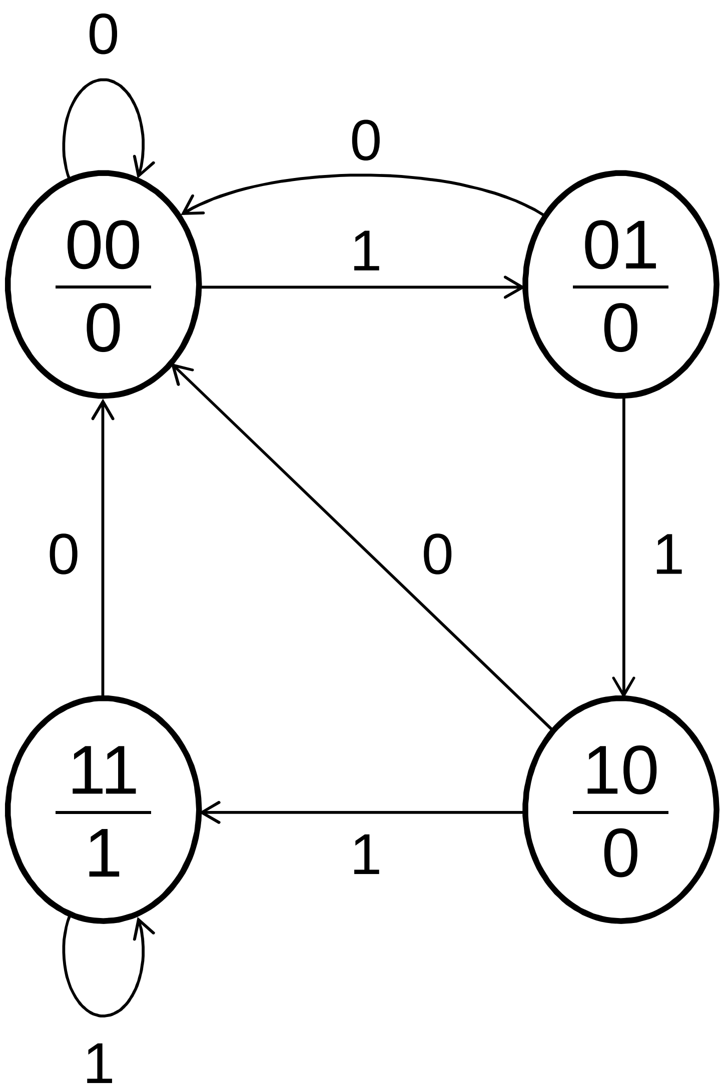
Moore Machine

- The outputs are a function of the Flip-Flop outputs only
- The outputs depend on the current state only
- The outputs are synchronized with the clock
- Glitches cannot appear in the outputs (even if inputs change)
- A given design might mix between Mealy and Moore



Moore State Diagram

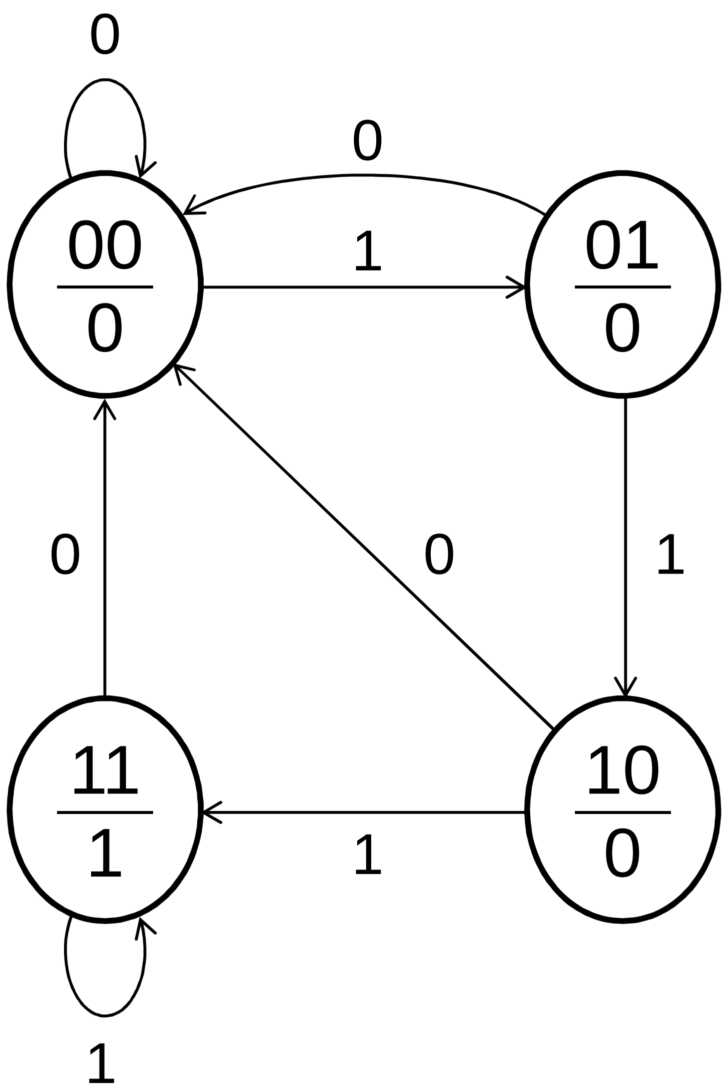
- ❖ An example of a Moore state diagram is shown on the right
- ❖ Arcs are labeled with input only
- ❖ The output is shown inside the state: (State / Output)
- ❖ The output depends on the current state only



Tracing a Moore State Diagram

- When the circuit is powered, the initial state (*AB*) and output are unknown
- Input *x* = 0 resets the state *AB* to 00. Can also be done with a reset signal.

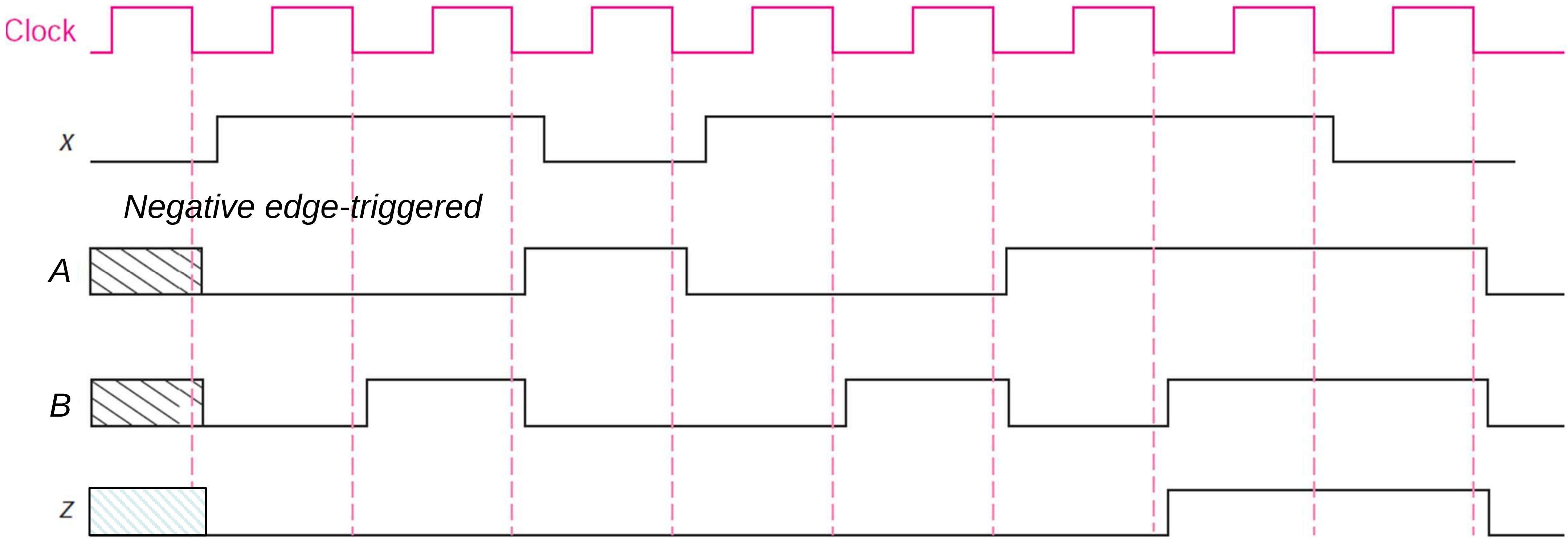
Cycle	**0**	**1**	**2**	**3**	**4**	**5**	**6**	**7**	**8**
Input *x*	0	1	1	0	1	1	1	1	0
Present State *A* *B*	?	0	0	1	0	0	1	1	1
	?	0	1	0	0	1	0	1	1
Output *z*	?	0	0	0	0	0	0	1	1



Timing Diagram of a Moore Machine

Cycle	0	1	2	3	4	5	6	7	8
Input *x*	0	1	1	0	1	1	1	1	0
Present State *A B*	?	0	0	1	0	0	1	1	1
	?	0	1	0	0	1	0	1	1
Output *z*	?	0	0	0	0	0	0	1	1

The output is synchronized with the clock. No false output (or glitch) can appear.



Summary

❖ To analyze a clocked sequential circuit:

1. Obtain the equations at the **Inputs** of the flip-flops
2. Obtain the **Next State** equations
   - For a D Flip-Flop, the Next State = D input equation
   - For T and JK, use the characteristic equation of the Flip-Flop
3. Obtain the **Output** equations
4. Fill the **State Table**
   - Put all the combinations of current state and input
   - Fill the next state and output columns
5. Draw the **State Diagram**

❖ Two types of clocked sequential circuits: **Mealy** versus **Moore**