EXPERIMENT 11

11. Traffic Light Controller

11.1 Objectives

- Practice on the design of clocked sequential circuits.
- Applications of sequential circuits.

11.2 Overview

In this lab you are going to develop a Finite State Machine (FSM) for a traffic light controller that will control the operation of traffic lights similar to the one at the KFUPM main gate. The crossing is shown in Figure 11.1.

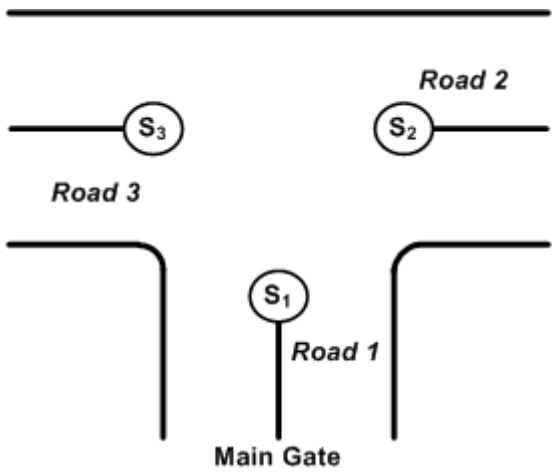

Figure 11.1: The Three Traffic Light Signals.

11.3 Design Specifications

There are three traffic light signals (S_1, S_2, and S_3), each alternating between two states, *RED* and *GREEN*. These signals control the traffic flow on the three roads, $road_1$, $road_2$, $road_3$ in four possible states as follows.

- In *STATE 1*, traffic coming through $road_1$. (S_1 = GREEN, S_2 = RED, S_3 = RED)
- In *STATE 2*, traffic coming through $road_2$. (S_1 = RED, S_2 = GREEN, S_3 = RED)
- In *STATE 3*, traffic coming through $road_3$. (S_1 = RED, S_2 = RED, S_3 = GREEN)
- In *STATE 0:* no traffic so give priority to the main gate's road. (S_1 = GREEN, S_2 = RED, S_3 = RED)

States 1, 2 and 3 are enumerated in Figure 11.2

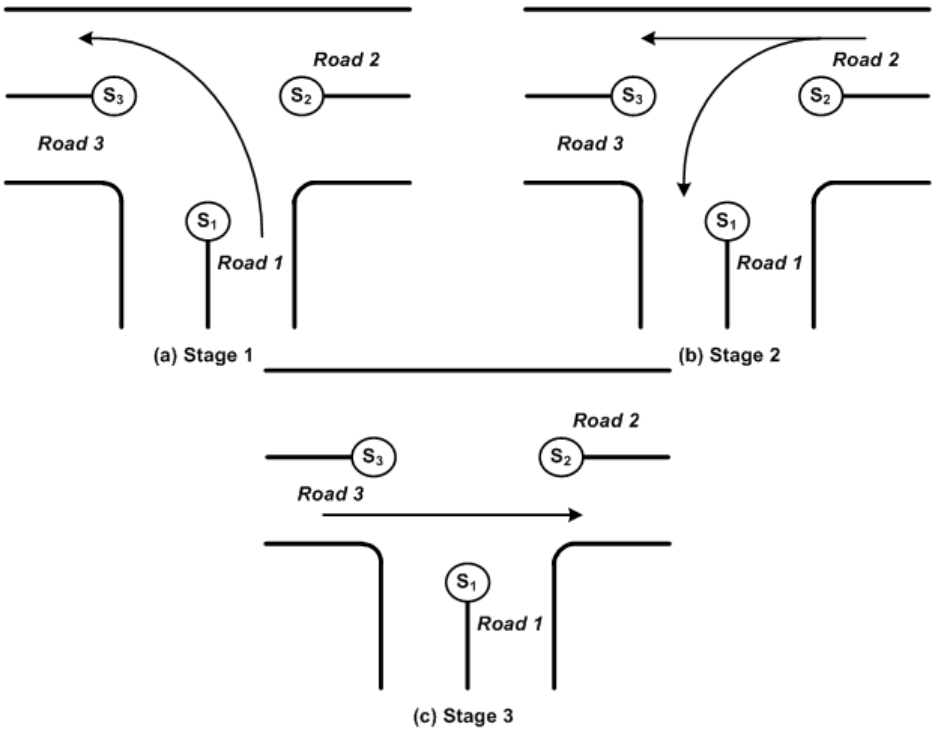

Figure 11.2: Traffic States.

The operation of the three light signals (S1, S2, and S3) is controlled through an arrangement of *traffic sensors* and *traffic light controller* circuit as shown in Figure 11.3**.** There are three traffic sensors x_1, x_2, *and* x_3, which sense the presence of traffic on the three roads as illustrated in Table 11.1. The controller operation is determined by the output of these three sensors as enumerated in Table 11.2.

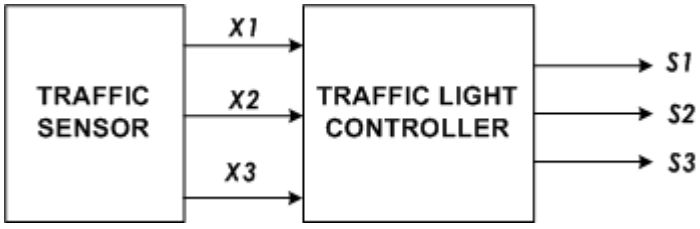

Figure 11.3: Traffic Sensor and Traffic Light Controller Circuit

Table 11.1: Traffic Sensor Signals.

x_3	x_2	x_1	Indication
0	0	0	No traffic for all roads
0	0	1	Traffic for $Road_1$ only
0	1	0	Traffic for $Road_2$ only
0	1	1	No traffic for $Road_3$
1	0	0	Traffic for $Road_3$ only
1	0	1	No traffic for $Road_2$
1	1	0	No traffic for $Road_1$
1	1	1	Traffic for all roads

Table 11.2: Traffic Sensors and Controller Operation.

x_3	x_2	x_1	Indication
0	0	0	Stay at STATE 0
0	0	1	Stay at STATE 1
0	1	0	Stay at STATE 2
0	1	1	Alternate between STATE 1 and STATE 2
1	0	0	Stay at STATE 3
1	0	1	Alternate between STATE 1 and STATE 3
1	1	0	Alternate between STATE 2 and STATE 3
1	1	1	Normal operation: STATE 1, STATE 2, STATE 3, STATE 1…

The design of the traffic controller module requires using D-Flip-Flops with asynchronous clear. Assume that the controller has three inputs: x_3, x_2, and x_1 coming from the traffic sensor, and three outputs: S_1, S_2, and S_3, which control the operation of the three traffic light signals (logic 1 represents a GREEN signal and logic 0 represents a RED signal).

11.4 Pre-Lab

- You are expected to know the design procedure of synchronous sequential circuit.
- Obtain either a state diagram or a state table for the circuit. In this case, it would be appropriate to get the state table directly (use the table below), whenever you have the choice to select between two states follow the order STATE1, STATE2, STATE3, then STATE1 and so on.
- Derive the Flip-Flop input equations from the state table.
- Derive output equations for the traffic signals.
    - A+=
    - B+=
    - S1=
    - S2=
    - S3=

No	X_3	X_2	X_1	A	B	D_A	D_B	S_3	S_2	S_1
0	0	0	0	0	0					
1	0	0	0	0	1					
2	0	0	0	1	0					
3	0	0	0	1	1					
4	0	0	1	0	0					
5	0	0	1	0	1					
6	0	0	1	1	0					
7	0	0	1	1	1					
8	0	1	0	0	0					
9	0	1	0	0	1					
10	0	1	0	1	0					
11	0	1	0	1	1					
12	0	1	1	0	0					
13	0	1	1	0	1					
14	0	1	1	1	0					
15	0	1	1	1	1					
16	1	0	0	0	0					
17	1	0	0	0	1					
18	1	0	0	1	0					
19	1	0	0	1	1					
20	1	0	1	0	0					
21	1	0	1	0	1					
22	1	0	1	1	0					
23	1	0	1	1	1					
24	1	1	0	0	0					
25	1	1	0	0	1					
26	1	1	0	1	0					
27	1	1	0	1	1					
28	1	1	1	0	0					
29	1	1	1	0	1					
30	1	1	1	1	0					
31	1	1	1	1	1					

11.5 In-Lab

1. In a new project, open a new schematic sheet and implement the functions that you have obtained in the pre-lab.
2. Use a D-Flip-Flops with Asynchronous Clear from the library.
3. Constrain the inputs of your circuit (x_3, x_2, and x_1) to 3 of the level switches (SW1, SW2, and SW3) respectively.
4. Constrain Flip-Flop outputs to LEDs (LD7 and LD8) where LD8 is the output of the least significant Flip-Flop. These will show the current state.
5. Constrain Flip-Flop inputs to LEDs (LD5 and LD6) where LD6 is the input of the least significant Flip-Flop. These will show the next state.
6. Constrain the three signal outputs (S_3, S_2, and S_1) to three LEDs (LD1, LD2, and LD3) respectively.
7. Use two Buttons, one to provide a clock signal (BTN1) -Beware of switch de-bouncing problems, and the other as an asynchronous clear (BTN4). Connect these inputs to the respective inputs of the Flip-Flops.
8. Download your design.
9. Verify its functionality by applying different input combinations and compare it with your state table.
10. Demonstrate your work to the instructor.

11.6 Post-Lab

- Document your design by providing a diagram of your circuit
- As a bonus propose a modification to your design that will take the following into account: If the circuit is alternating between different states (for example if $x_3\, x_2\, x_1 = 1\ 1\ 1$), each state should remain no more than 10 sec before moving to the next state and so on.