Lab # 8

An Alarm Clock – Phase 2

Objectives

- Practice using the K-map simplification method
- Designing a BCD to seven-segment display decoder.

Overview

A seven-segment, like the one shown in Figure 8-1, is a common output device used in many digital applications like timers. The seven-segment is so called because of the seven LEDs, or segments, it is composed of. There are two types of seven segment displays, common anode and a common cathode seven-segment display. In either case, one end, either positive or negative, of all the seven segments are connected together to a common pin. The seven-segment in which positive end of all the segments are joined together to a common terminal is referred as a common anode seven segment. On the contrary, common-cathode seven-segment display has negative terminals of its seven-segments connected to a common node. To light a segment in the seven-segment display, the common terminal is first connected to logic high for common anode or to logic low for common cathode. The other ends for individual segments are then connected to logic low for common anode and logic high for a common cathode type seven-segment display.

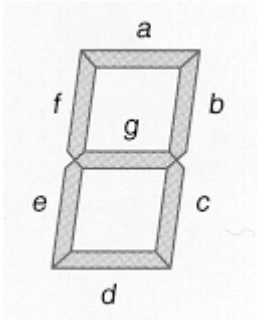

Figure 8-1: Seven-Segment Display

The Digilab provides four common-anode type seven-segment displays. The common anode for the first seven-segment display is called A1; A2 for the second display, and so on. The segments of each display are called *a, b*, up to *g* as shown in Figure 8-1. In order to reduce the number of connections needed on the board, the cathode pins from each display have been connected together to form *seven common terminals*, called a, b, c, d, e, f and g, corresponding to the seven-segments. Thus to illuminate a segment of a particular display, e.g. segment *e* of the third display, one needs to apply a "1" (High or Vdd) to anode A3 (to first select the segment A3) and a "0" (GND or Low) to cathode node *e* (to light segment e).

The pin connection for seven-segment display available on the FPGA board is given in Table 1.

Table 1: Seven Segment Pin Connections

Seven-segment Terminal	Pin # of FPGA	Pin on J1 connector
A1 (Anode digit 1)	44	A1
A2 (Anode digit 2)	40	A2
A3 (Anode digit 3)	39	A3
A4 (Anode digit 4)	38	A4
A (Cathode of segment A)	51	CA
B	50	CB
C	49	CC
D	48	CD
E	47	CE
F	46	CF
G	45	CG
Dec. point	-	DP

A BCD to seven-segment display decoder is a combinational circuit that accepts a BCD digit as input and generates appropriate outputs for enabling/disabling each of the 7 segments so as to display the corresponding decimal digit. The decoder has seven outputs (*a*, *b*, *c*, *d*, *e*, *f*, *g*) each output controls the corresponding segment in the 7-segment display as shown below.

For example, for a zero to be displayed, all segments should be enabled with the exception of segment-*g*, which should be disabled.

Design Specifications

You need to design a BCD decoder that accepts a BCD code and outputs the seven segments states that correspond to the supplied BCD number.

Pre-Lab

A partially filled truth table for the circuit is given in Table 2. Complete the table by filling in the values for the seven outputs so that the circuit will display the correct decimal digit when the input lines supply the corresponding BCD code.

Note that since we have a common-anode type seven segment display, so for a segment to be ON, it should be connected to the GND, as illustrated for segment-a in Table 2.

Decimal digit	Inputs				Outputs						
	D	C	B	A	a	b	c	d	e	f	g
0	0	0	0	0	0						
1	0	0	0	1	1						
2	0	0	1	0	0						
3	0	0	1	1	0						
4	0	1	0	0	1						

5	0	1	0	1	0						
6	0	1	1	0	1						
7	0	1	1	1	0						
8	1	0	0	0	0						
9	1	0	0	1	0						
10	1	0	1	0	X						
11	1	0	1	1	X						
12	1	1	0	0	X						
13	1	1	0	1	X						
14	1	1	1	0	X						
15	1	1	1	1	X						

Invalid Input Combinations

Table 2: Truth table of the BCD-to-seven-segment display decoder.

Use K-Maps to simplify each segment function. You should come to the lab with the simplified Boolean equation of every segment.

In-Lab

- In a new schematic sheet, build a macro for the above BCD to seven-segment display decoder. The macro should accept a BCD (4 bits) as input. Constraint the outputs of this macro to the seven-segments directly.
- Open your previous lab schematic. Connect the 4 outputs of the minutes counter (the least significant digit) to the inputs of the BDC decoder macro you have built in step 1.
- Constrain the anode of the 7-seg display you have chosen to the VDD, and constrain the anodes of the other to GND.
- Download your design.
- Verify its functionality by pushing the AM button and observing that the least significant digit of the minutes counter is incremented with every push. Demonstrate your work to the lab instructor.
- Next you are required to display the least significant digit of the hours counter on one of the displays. Demonstrate your work to the lab instructor.

Post-Lab

- Document your design by providing a diagram of the BCD to seven-segment display decoder.
- As a **bonus**, propose an idea to display two digits simultaneously on two displays.