Lab # 3

The Software

Objectives

1- Familiarize with FPGA board.
2- Familiarize with FPGA design steps & tools.
3- Familiarize with FPGA board.
4- Binding inputs and outputs to certain switches and LEDs.
5- Derive & verify the 2^n-rows T. table of the function.

Description

- Introduce FPGA (CLB's, Programmable IO Pads, Input Buffers, Output Buffers, Clock Pin, Clock buffer)
- FPGA design steps and tools.
- FPGA board (switches, push buttons, LEDs & power supply pins. 7-Seg, Display, etc.)
- Design tools: schematic capture, functional simulation, download configuration bits
- Given a 4-variable logic diagram of basic gates (which has several similar repeated sub-circuits), students should:
    - Derive/anticipate the truth-table of the output function
    - Draw the schematic diagram and simulate the function.
    - Implement the circuit and verify the truth-table

Pre-lab

- Read the introductory section to get familiarized with the software.
- Find the truth table for the circuit given in Figure 4.1 for the primary outputs and at the wires F1 and F2.

In-lab

The lab requires you to go through all the stages of the design process using Xilinx and Digilab tools. You will be designing and functionally testing your design in Xilinx CAD software. Then you will verify your design on the board as well.

This being your first lab, the steps of the design are detailed as under. You may like to refer to lab guide for details on how to perform individual steps.

- Start the Xilinx project manager, configure the device and name the project as lab3.
- Create schematic for the lab.
    - Start by selecting a new schematic.
    - Add the symbols for the gates needed for the circuit in Figure 4.1
    - Place three input pads, IPAD, followed by input buffers, IBUF, and constrain them to three input switches (SW8, SW7 and SW6).
    - Place two output pads, OPAD, succeeded by output buffers, OBUF, and constrain them to two LEDs (LD8 and LD7).
    - Name the input and output nets. Your schematic would look like Figure 4.1
    - Perform an integrity test. Check to see f there are any errors or warnings and remove them.
- Design Simulation
    - Start the simulator and add the input/output signals
    - Assign counter the eight possible combinations and watch the signal at the primary outputs (SUM and CARRY) and at checkpoints F1, F2.
    - Simulate the design in steps as shown in Figure 4.2
- Verify functionality of the design.
- Implement the design
    - Download the design on Digilab board
    - Verification

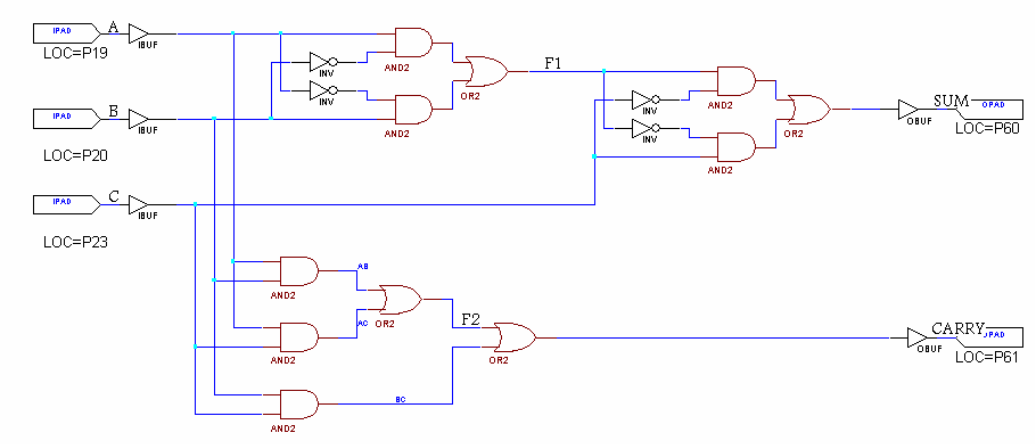

Figure 4.1

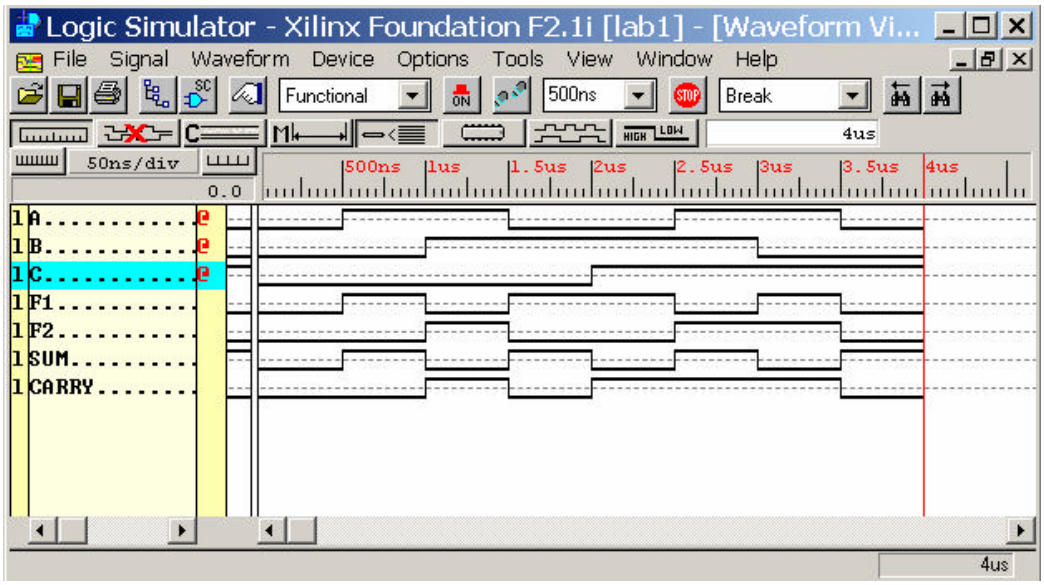

Figure 4.2