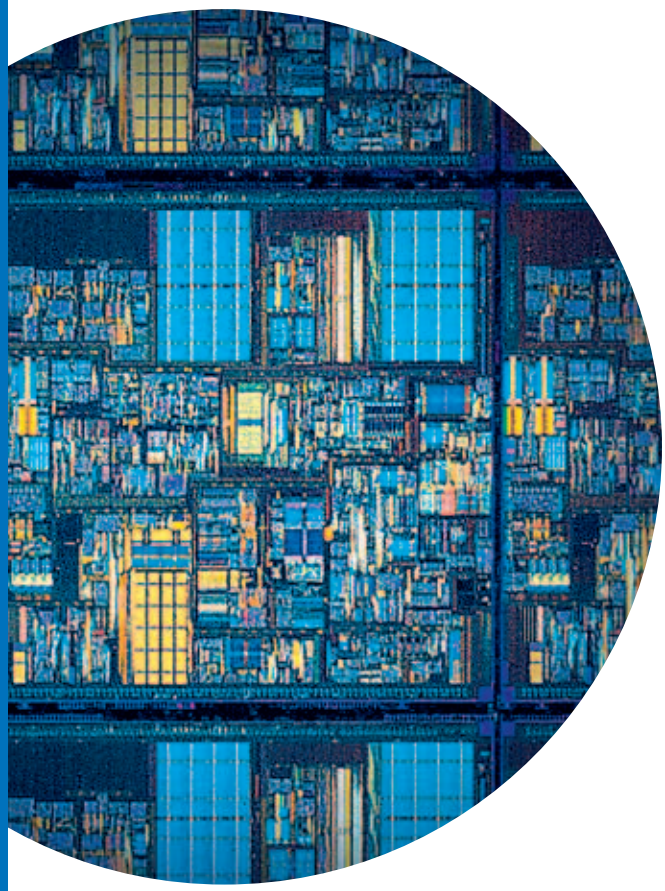
Designing for Power

Intel Leadership in Power Efficient Silicon and System Design



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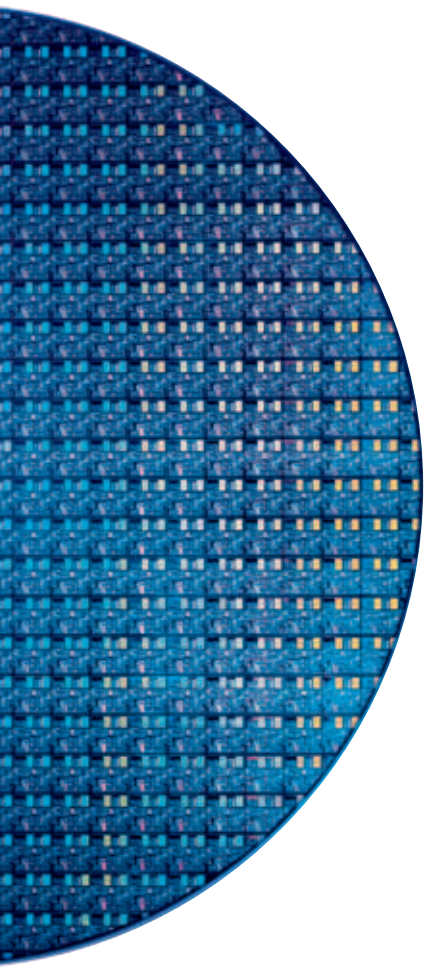


The Power Challenge

More than a quarter century ago, Intel co-founder Gordon Moore forecasted the rapid pace of technology innovation. His prediction, popularly known as "Moore's Law," states that transistor density on integrated circuits doubles every two years. Today, Intel continues to apply the principles of Moore's Law, achieving higher levels of integration and producing a steady stream of smaller, faster, cheaper chips, bringing exponential growth in computing and communications technology to consumers and businesses worldwide.

Demand Increases

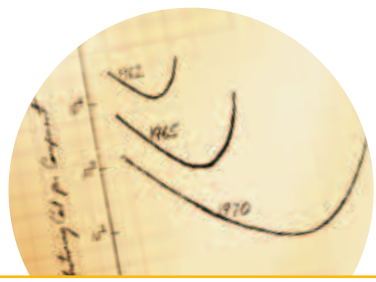
As computing and communications converge and pervade nearly every aspect of life, the demand increases for devices with more functionality, faster operation, and lower costs. Keeping pace with Moore's Law is essential to help computing and communications industries deliver chips that meet these needs.

However, as more transistors are integrated on a chip to enable more functions, and higher frequency is used to obtain increased performance, total power consumption increases and results in more heat. As more transistors are packed into a smaller area, the power density also increases. Consumers' desire for mobility and multifunctional small form factor devices places additional challenges like efficient battery operation.

Power Management

Efficient power and thermal management are vital as systems become smaller or more capable with every generation of Moore's Law. Power must be delivered and used efficiently by the chips, wiring, and display, while effectively dissipating heat from the system – economically, of course.

Addressing the power challenge allows a continuation of the trend toward smaller, faster, cost effective chips and devices. As a result, futuristic applications that require more powerful processors may be realized. Increasing capability and density of computing and communications chips may be sustained. Comprehensive power and thermal management techniques are a fundamental part of continuing to receive the benefits of Moore's Law.



Moore's Law states that the transistor density on integrated circuits doubles every two years. Today, adding transistors on pace with Moore's Law continues to drive increased functionality, performance and decreased cost of computing and communications technology.

Designing for Power

Intel was one of the first companies to anticipate the trends and clarify the scope of the power challenge faced by the computing and communication industry. With multiple innovative solutions, Intel is leading the industry in addressing the challenge successfully and is working with many other companies and organizations that have joined in the challenge of designing for power.

A Holistic Approach

Intel researchers, scientists, and engineers take a holistic approach to power and thermal management. Intel engineers examine every aspect of the design, manufacture, and use of computing devices, looking for variables that could influence the power equation. Intel is exploring new process technologies, breakthrough transistor materials and structure, innovative circuit and microarchitectural designs, novel packaging materials and techniques, improvements to system components and software optimization techniques that provide comprehensive power efficient solutions.

Intel is no stranger to the challenge of maximizing performance while minimizing power. Intel has designed power-efficient solutions for mobile PCs for more than a decade. Back in the 1980s, Intel switched its process technology from NMOS to CMOS to better manage the power requirement. Intel has been able to keep pace with the Moore's Law trajectory by leading the industry with world-class process technology innovations. Now that power has become a key differentiator for devices of all sizes and types, we are applying our experience to address the full range of computerized systems, from cell phones to servers.

Maximizing Power Efficiency

Raw processing performance is only one of several key vectors that will define future innovation in micro-architectures and circuit design. The next decade will see a number of architectural changes at every level, from transistor structure to integration of entire systems, which will continue to drive to a key goal: to maximize power efficiency at every phase of the design. This brochure highlights the industry leading technologies being developed and deployed by Intel to meet the challenges of designing for power.

"We must develop innovative approaches to managing power at the circuit and microarchitecture level if we are to continue fulfilling the promise of Moore's Law."

Justin Rattner
Intel Senior Fellow,
Senior Director, Microprocessor Technology Lab

Addressing Power at the Transistor Level

Intel is a world leader in silicon process technology and volume manufacturing capabilities. By drawing on that expertise, Intel continues to address the challenges posed by power by reducing transistor leakage as well as active power associated with interconnect resistance and capacitance.

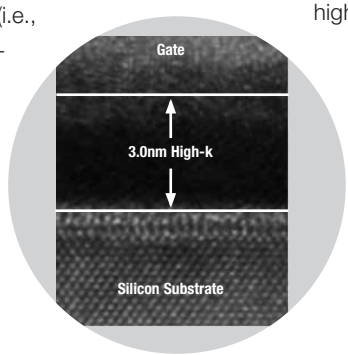
New Process Technology

Intel has kept pace with Moore's Law by introducing a new generation of process technology every two years; this has been the fundamental enabler of cheaper, faster, better products to consumers. In August 2004, two years after 90 nanometer (nm) process technology was first introduced, Intel showcased its next-generation 65 nm (65 billionths of a meter) process technology, the world's most advanced process for chip manufacturing. The 65 nm process technology allows printing of individual circuit lines smaller than a virus and creation of transistor gate widths of only 35 nm. These extremely small and fast transistors are the building blocks of high-speed microprocessors. However, as transistors shrink, leakage current can increase and managing that heat is crucial for reliable high-speed operation. This is becoming an increasingly important factor in chip design.

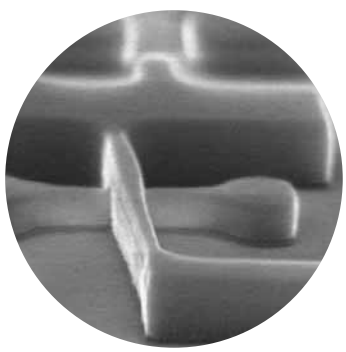
In the 90 nm process technology, Intel helped address part of the challenge by introducing strained silicon. Intel's proprietary "Uni-axial" strained silicon reduced leakage current by five times or more without diminishing performance (i.e., on-current). Similar techniques result in greater savings in leakage current as Intel scales to the 65 nm process, as Intel's second-generation strained silicon reduces leakage current by another four times or more. Reduced leakage current means better power efficiency and less heat dissipation per transistor.

Intel introduced copper interconnects in the 130 nm process technology to lower resistance. Carbon-Doped-Oxide (CDO) was first introduced in Intel's 90 nm node to lower interconnect capacitance. Lower resistance and capacitance both decrease power requirements. Intel has developed a second-generation CDO for its 65 nm node with even lower capacitance.

The 65 nm process technology has an extra metal interconnect layer that improves density and performance, enhancing power and clock distribution as well as all the signals on the chip.



Future High-k Dielectric for Reduced Gate Leakage



Intel 30nm Tri-gate Transistor

Transistor Material and Structure

Intel continues to research new power-efficient transistor materials and structures that might be used in future process technologies.

Hi-K Dielectric and Metal Gate

Transistors act as silicon-based switches that process the ones and zeros of the digital world. A gate electrode turns the transistor on and off, and a gate dielectric is an insulator beneath it. The voltage of the gate electrode above it controls the flow of electric current across the transistor. The gate dielectric (currently made of silicon dioxide) thickness in a 65 nm transistor is 1.2 nm, which is represents a thickness of only five atomic layers. Silicon dioxide has been used as a dielectric for almost three decades.

However, as silicon dioxide gets thinner, electric leakage current through the gate dielectric increases and leads to wasted current and unnecessary heat. To keep electrons flowing in the proper location and greatly reduce this critical source of heat, Intel plans to replace the current material with a thicker so-called "high-k" material, significantly reducing current leakage. The high-k material has 100 times less leakage than silicon dioxide. Since this new gate dielectric is not compatible with today's transistor gate electrode material, Intel developed a new metal gate technology, allowing this process to be suitable for high volume manufacturing. These new discoveries can be integrated into an economical and high-volume manufacturing process to address the power and heat increases in smaller nanostructures.

Tri-gate Transistor Structure

Intel has also developed a novel three-dimensional design that will allow the manufacture of transistors that scale, perform, and address the current leakage problem seen in smaller dimension planar transistors. Tri-gate fully-depleted substrate transistors have a raised plateau-like gate structure with two vertical walls and a horizontal wall of gate electrode. This three-dimensional structure improves the drive current while the depleted substrate reduces the leakage current when the transistor is in the "off" state. Reducing the leakage current in the off state not only helps control heat at the circuit level but also translates to increased battery life in mobile devices.

Meeting the Challenge Through Chip Design

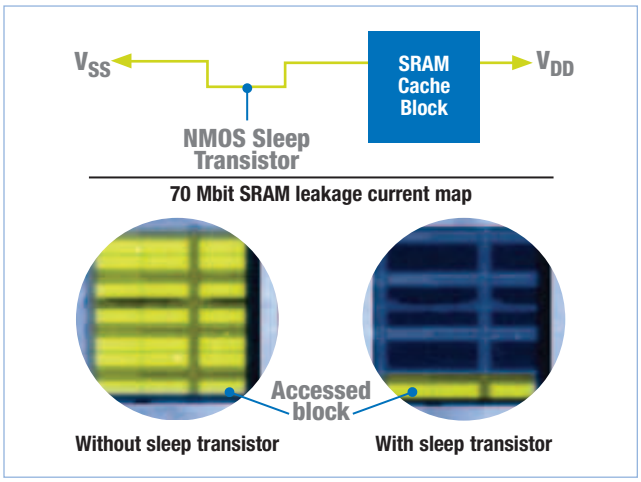
Intel is also tackling power challenges at the chip level through innovations in circuit and micro-architecture research and design.

Leakage Control Through Body Bias and Sleep Transistor

Intel researchers are developing low-power circuit design techniques for microprocessors as feature sizes fall below 100 nm. As feature sizes decrease, transistors leak power, even when they are turned off. Controlling power leakage is an important design consideration in future generations of microprocessors.

Intel is testing a number of these techniques on a prototype Arithmetic Logical Unit (ALU). By dynamically adjusting the voltage applied to the body of a transistor (bias), researchers can manipulate the transistor's threshold voltage – the voltage at which the transistor turns on. Increasing the threshold voltage reduces the leakage but also reduces performance. Having localized control of the bias voltage enables the designer to make real-time trade-offs between the circuit performance and power it consumes. This capability can be used to reduce leakage during periods of inactivity or to increase performance during peak use.

The Dynamic Sleep Transistor is another innovative technique that adds a transistor in series with the power supply that can be turned off when a block of logic circuitry is in idle mode, thus reducing leakage. The Sleep Transistor-based power saving feature is expected to be introduced in Intel's 65 nm process technology products. For example, a large portion of 65 nm microprocessors is occupied by Static Random Access Memory (SRAM), which is used to cache data and instructions. The Sleep Transistors can shut off large blocks of idle SRAM to eliminate wasted power. **Power efficient larger sized caches could improve performance by increasing the data bandwidth and reducing latency.**



Power-aware Multi-everywhere Microarchitecture

Intel's microarchitecture researchers are exploring new architectures that are "conscious" of power and thermal challenges and able to manage them dynamically while running applications. Intel is investigating multi-core based microprocessors, clustered micro-architectures, and other power-optimized microarchitectures.

Multi-core, Multithreaded and Clustered Microarchitectures

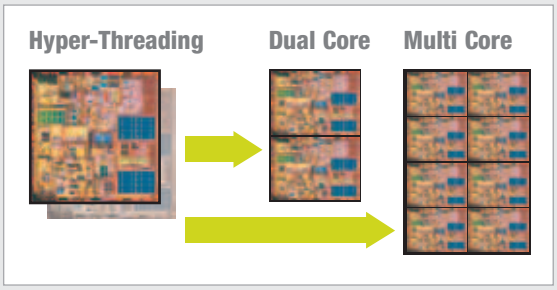
Intel is implementing dual-core microarchitectures and examining the concepts of clustered microarchitectures to increase overall performance while managing power more effectively. This unique approach focuses on CPU cores and clusters that perform optimized load balancing through a combination of software and hardware mechanisms that dynamically examine the utilization, priority, and thermal characteristics of a workload. As a result, **Multicore with Multithreading architecture can increase the performance without significant increase in either the baseline frequency of operation or the net power consumption of the device. This technique provides the flexibility for each core to run at different frequency or voltage. Core hopping mechanisms can be used to spread the power dissipation over a greater area, and some of the cores could be dedicated for special purpose operation to achieve power efficient performance increase.**

Power-optimized Microarchitecture

Intel microprocessors include innovations and instruction set extensions that provide more performance for less power by squeezing more useful activity into each machine instruction. Intel continues to strive to eliminate redundancy at the microarchitecture level by identifying frequent instruction sequences, extensively optimizing them, and storing them for later reuse. Intel NetBurst® microarchitecture has an advanced form of an instruction cache called the Execution Trace Cache, which stores the already decoded machine instructions or micro-ops for future reuse. Hyper-Threading Technology, available in the Intel mobile and server processors, increases performance without significantly impacting the power envelope.

Enhanced Intel SpeedStep® Technology

The Enhanced Intel SpeedStep® Technology dynamically scales frequency and voltage according to how much processing power is needed, significantly extending battery life in mobile systems and reducing usage power in desktop and server systems. Demand based Switching is a server version of this technology and is being deployed in the Intel® Xeon™ and Itanium® 2 product lines. We are exploring the possibility of extending this technology to other system components as well, to further reduce overall power consumption.



Low Power with Dual-core and Multi-core Architectures

Intel is at the forefront of addressing power challenges by designing chips that balance power, performance, functionality and cost; the ground work for which was laid decades ago with the vision of Moore's Law. Today, Moore's Law continues to benefit function, power, performance and cost. Intel's industry leading process technology produces chips that integrate billions of transistors. These transistors are used to provide consumers with increased functionality and flexibility through power-efficient platforms like Intel® Centrino™ Mobile Technology and power-efficient technologies that improve performance such as Hyper-Threading Technology (HTT) from Intel.

HTT, integrated into Intel® Xeon™ processor family server products and Intel® Pentium® 4 desktop products, enables two independent threads that allow one physical processor to appear and behave as two virtual processors to the operating system. HTT allows an increased number of applications to run more seamlessly together, like simultaneously CD burning, video streaming and virus scanning, all with uncompromised performance and power efficiency.

HTT was conceived as a seed vehicle for a future vision of multi-everywhere computing architectures. Intel's Dual Core microprocessors, expected in 2005, are continuation of this vision. Further more, improved process technologies like 65 nm process technology would enable larger numbers of transistors to be integrated in a given die size. Enabling processes and techniques that allow integration of additional transistors into existing power envelopes allows creative decisions on what to do with the additional transistors. Key directions Intel could be spending this increased transistor budget are new low-power architectures such as multi-core – where multiple microprocessor cores are integrated onto a single chip – or new innovative features such as virtualization and security capabilities – allowing higher levels of trust and robustness in computers.

Developing System Solutions

To address power challenges at the system level, Intel strives to improve the power profile of its own components, help component manufacturers and system designers better manage power, and collaborate with others in the industry to develop broader solutions. Intel focuses on the full range of systems, from cell phones and Personal Digital Assistants (PDA) to notebook computers, desktop PCs and servers.

Packaging Solutions for Heat Dissipation

Intel invests considerable resources in packaging-related research and development to move heat away from the silicon surface itself. One innovation being explored involves eliminating the bumps of solder that make the connections between the package and the chip. This small change would reduce the packaging thickness, thereby enabling the processor to run at lower voltage and allowing for thinner form-factor devices. Intel also remains committed to investigating various heat spreaders and packaging materials that will target hotspots and efficiently remove heat from the die.

System Component Solutions

Intel systematically studies the components of all types of systems, from cell phones to servers, to identify where and how power can be reduced or managed more effectively to improve the overall power performance of the system.

Improved Voltage Regulation

For notebook customers, Intel developed Intel® Mobile Voltage Positioning (IMVP) technology, to optimize voltage regulation for the Mobile Intel® Pentium® 4 processor. Intel also created Dynamic Voltage Management technology, to enable developers of components for microprocessors as well as wireless and handheld products to scale frequency and voltage dynamically, adjusting performance to application needs. In addition to improving their own designs, Intel advises power component suppliers on how to design more efficient voltage regulators, also strives to move the industry towards lower voltages on commodity components, such as Flash and DRAM.

Improved Display Power Specs

Intel works with the manufacturers of LCD displays to improve the efficiency of the electronics that drive the backlight. Optics experts also provide recommendations to the industry on how to design for greater power efficiency in passing light to the front of the display. For wireless and handheld devices, Intel is helping to drive to an industry standard for very low signal swing serial interface for displays, which potentially could reduce power loss across the interface by an order of magnitude.

Thermal Design and Engineering

To improve heat dissipation, Intel enables new heat sink technologies for our processors as well as focusing on other system components that must be cooled, such as graphics controllers and chipsets. Intel enables new chassis designs by building system models and running airflow analysis on them to improve airflow and cooling. In small form-factor platforms, thermal profiling identifies power hotspots in the system design early on when it is more cost-effective to make changes to address thermal challenges.

Intel continuously provides design ideas to original equipment manufacturer (OEM) and original design manufacturer (ODM) customers as well as other enclosure manufacturers to help them achieve more effective thermal design and engineering. Intel also engages the industry in developing new solutions through public presentations, course offerings on thermal design and engineering, and promoting standards such as SSI (Server System Infrastructure) that would increase the power efficiency of chipset and board layouts.

Intel is working with the National Resources Defense Council (NRDC) and the U.S. Environmental Protection Agency (EPA) to institute industry-wide acceptance of new power supply guidelines intended to reduce the overall power consumption of desktop PCs. These efforts have not gone unnoted – the EPA presented Intel the EPA 2004 Energy Star Award for work on the new guidelines. The power efficient guidelines enable quieter and small form factor PCs that consume less energy.

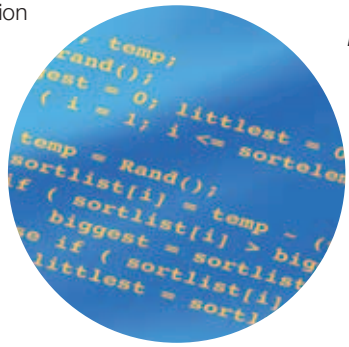
Active and Idle State Power Management

Power management has two vectors: reducing active, or "in use," power consumption and reducing power consumption when a device is in an idle state. Intel is researching adaptive, context-aware system-level power management policies to aggressively identify which system components are not being used during an active state and put them in the lowest possible power state without user intervention. The focus in idle state power management allows keeping the vital functionality of a small factor device active while the rest of the device is in "sleep" mode, thereby reducing active power. Intel researchers are developing a low-power state we call hypernate, which will achieve power saving close to Advanced Configuration and Power Interface (ACPI) "suspend to disk" mode but with much lower resume latency.

Optimization Strategy for Data Center

As utility costs increase and higher density platforms become available, it becomes more and more important to develop technologies and operational strategies that improve power and thermal control at the rack and data center levels. Intel is developing two concepts called Pconfig and Power Supply Management Interface (PSMI) that give the IT industry ways to better manage data center rack density.

Using Pconfig, the maximum power load based on the configurations of the systems in the rack can be calculated. PSMI allows tracking of actual power consumption using a console manager. By using power supplies with monitoring capabilities, IT can track the server usage to provide additional safety margin with Pconifg, and also interact with the Heating, Ventilation and Air conditioning (HVAC) systems to achieve more effective thermal efficiency within the data centers.



"There's a great deal that software can contribute to making a system manage power more effectively. We have created tools to help developers understand how their software can help or hinder power efficiency. They can use our tools to develop software that will enable systems to run on less power and perform more power-efficiently."

Richard Wirt
Intel Senior Fellow,
General Manager, Software
and Systems Group

Reference Solutions

To help OEMs create power-efficient systems, Intel builds a variety of reference designs. These hardware models include recommendations for where to locate the processor, memory, heat dissipation technology, and other components to optimize the power efficiency of the system.

Software Solutions

Intel's holistic approach to addressing the power challenge also extends to software. By offering developers tools such as the Intel® VTune™ performance analyzer, which optimizes software code so that it takes less time to execute a given task, overall power consumption is lowered. Intel makes recommendations to component manufacturers on how to minimize common programming errors that prevent the operating system from managing power effectively, and also encourages application software developers to modify their programs to enable users to trade off application qualities in favor of saving power. Mobility software-enabling collateral shows developers how to optimize their applications to improve user experience and extend battery life.

Intel research and development is a decentralized worldwide network of researchers, scientists, and engineers who are pioneering technology innovation and catalyzing cooperation within the computing and communications industry. With a network of more than 7,000 technology professionals, Intel can focus on developing breakthroughs in a variety of areas, including silicon technology and manufacturing, microarchitecture and circuits, computing platforms, communications and networking, and software technology. For more than 30 years, the company's research and development activities have continually expanded the possibilities for enhancing people's lives and work through computing and communications.

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