Slide 1

ITCS 4141/5141 Computer Organization and Architecture

Summer 2002

Barry Wilkinson
Department of Computer Science
University of North Carolina at Charlotte

Monday/Tuesday/Wednesday/Thursday/Friday
3:00 pm - 4:30 pm
Kennedy 135

Slide 2

Course

The course is concerned with design techniques for high performance computer systems. This course continues the topics of ITCS 3182 in more detail and explores advanced topics such as superscalar design. Other topics include the organization of the main/disk memory hierarchy and an introduction to multiprocessors.

Slide 3

Course Text

Not strictly necessary as on-line slides will be provided on home page. For reading:

Barry Wilkinson, *Computer Architecture, Design and Performance 2nd Edition*, Prentice Hall 1996.

Also see:

D. A. Patterson and J. L. Hennessy *Computer Architecture A Quantitative Approach 2nd edition*, Morgan Kaufmann, 1996

D. Sima, T. Fountain, and P. Kacsuk, *Advanced Computer Architecture A Design Space Approach*, Addison-Wesley, 1997.

Slide 4

Prerequisites

ITCS 3182 (see http://www.cs.uncc.edu/~abw/ITCS3182/) or equivalent or consent of department.

Anyone without the prerequisite who continues to be registered in this course will receive an F/U grade for dishonesty. If there is any doubt, please obtain a written note from the dept/instructor.

ITCS 5141 IS A SECOND COURSE ON COMPUTER ORGANIZATION, AND HENCE BASIC KNOWLEDGE OF COMPUTER ORGANIZATION IS EXPECTED.

Knowledge of C and an assembly language are also assumed.

Slide 5

Home page

For materials, assignments, announcements, etc.

http://www.cs.uncc.edu/~abw/ITCS5141/

Please check this page before each class.

Slide 6

Course Outline

Broadly three parts, a review and discussion of ITCS 3182 material, further study of these topics (pipelined design, cache memory and memory management), and finally a detailed study of higher performance superscalar and multiprocessor systems:

- Review of the stored program concept
- Detailed study of pipelined processor design
- Cache memory
- Memory management
- Higher performance processor design
- Shared memory multiprocessor systems

Slide 7

Assessment

Class tests (2)	40%
Project/assignments	40%
Final exam	20%

All submitted assignments must be your own work. Copied work or work done by more than one person (unless specifically instructed) will not be accepted. No work will be accepted after the due date without a good reason. No make-up tests.

Attendance - expected. If you miss classes, it will have a deleterious effect on your grade. Attendance will be taken.

Slide 8

Instructor

Barry Wilkinson

Room: Kennedy 214

Tele: 687 4879

Email: abw@uncc.edu

Office Hours

Monday/Tuesday/Wednesday/Thursday/Friday: 4:30 pm onwards.

Please come at 4:30 pm as I will not wait if no one there.

Lecture 1

Processor Design

Review of Stored Program Concept

Stored Program Computer

Has a list of binary encoded instructions held in a memory (stored program) that define the actions of computer.

Consists of:

- Memory
- Processor
- Input circuits and devices
- Output circuits and devices

Processor fetches (machine) instructions from memory and performs actions defined.

Slide 11

Babbage

Concept first proposed by Babbage in the 1800's - his machine was mechanical but had the main parts of a modern computer; an arithmetic unit and controller (processor), memory (punched cards) - never completed because the mechanical complexity (gears etc).

Slide 12

1930 - 40's

Atanasoff-Berry Computer (ABC) - John Atanasoff at Iowa State College. (Berry was a research assistant.)

Special purpose digital computer for solving linear algebraic equations. Not widely known until patent litigation over ENIAC in 1967-69.

Z3 - Konrad Zuse, Germany - relay machine.

Destroyed by bombing raid on Berlin.

Instructions of form:
R2 = R1 <operation> R2.

Eleven operations.

No conditional branch operations.

Loops could be done with loop of punched film.

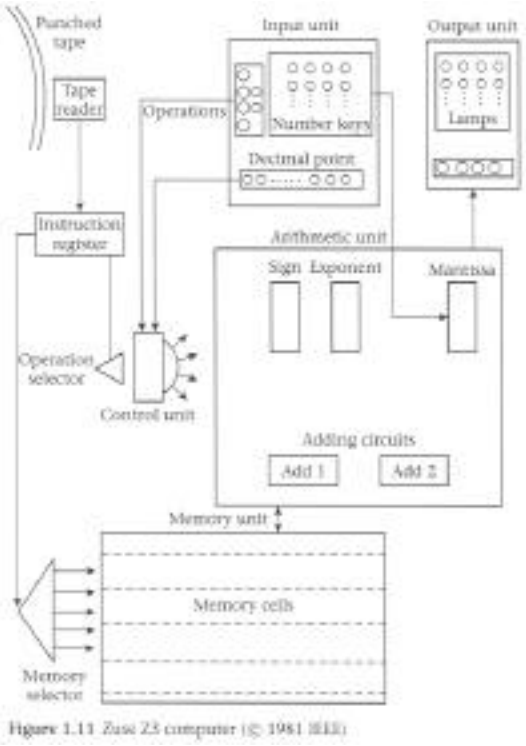


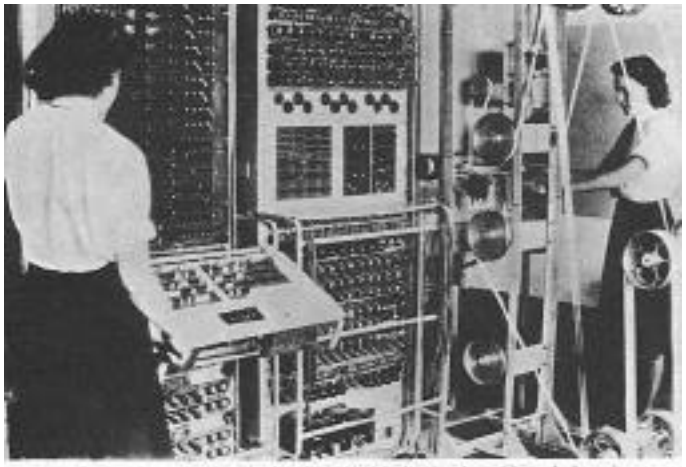
Figure 1.11 Zuse Z3 computer (© 1981 IEEE)

Source: *Computer Architecture and Implementation* by H. G. Cragon, Cambridge University Press, 2000.

Colossus

British Government - for breaking enciphered German messages.

First operational 1943. Ten built. Kept secret until 1975.



The Colossus in operation at Bletchley Park, 1944-5, showing the rapid punched tape input mechanism.

Source of picture “Alan Turing the Enigma” by A. Hodges, Simon and Schuster, 1983. Should be compulsory reading for all CS majors.

Harvard Mark 1

Howard Aiken Assistant professor Harvard University proposed a machine for to produce tables of functions.

Approached IBM who built the machine.

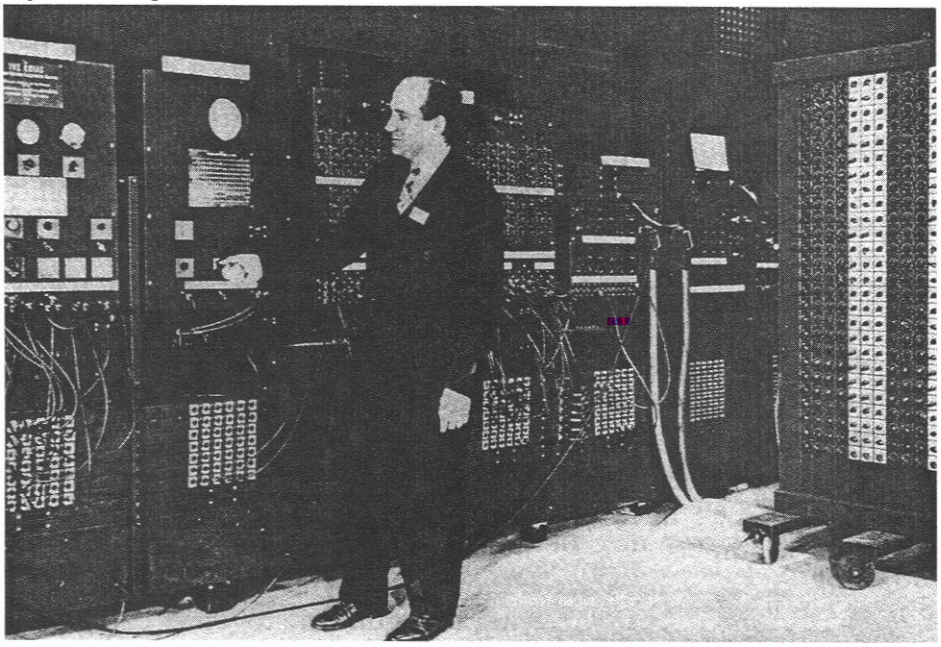
Electromechanical (not electronic). Used IBM's technology in punched card machines and tabulators. Program stored on punched tape.

Operational 1943 - 1959.

ENIAC project

Electronic Numerical Integrator and Computer

Hugh electronic computer (over 18,000 vacuum tubes) developed during World War II - did not have stored program (programming done by setting switches.



ENIAC with Eckert. Program entered using switches on lower part of equipment

Slide 17

EDVAC project

Electronic Discrete Variable Computer

Proposed towards end of ENIAC project - Eckert, Mauchly and von Neumann - Report (published with one name, von Neumann) on the design of an electronic stored program computer.

Slide 18

von Neumann computer

Describes a stored program computer that uses the memory to hold both binary encoded instructions (program) and data.

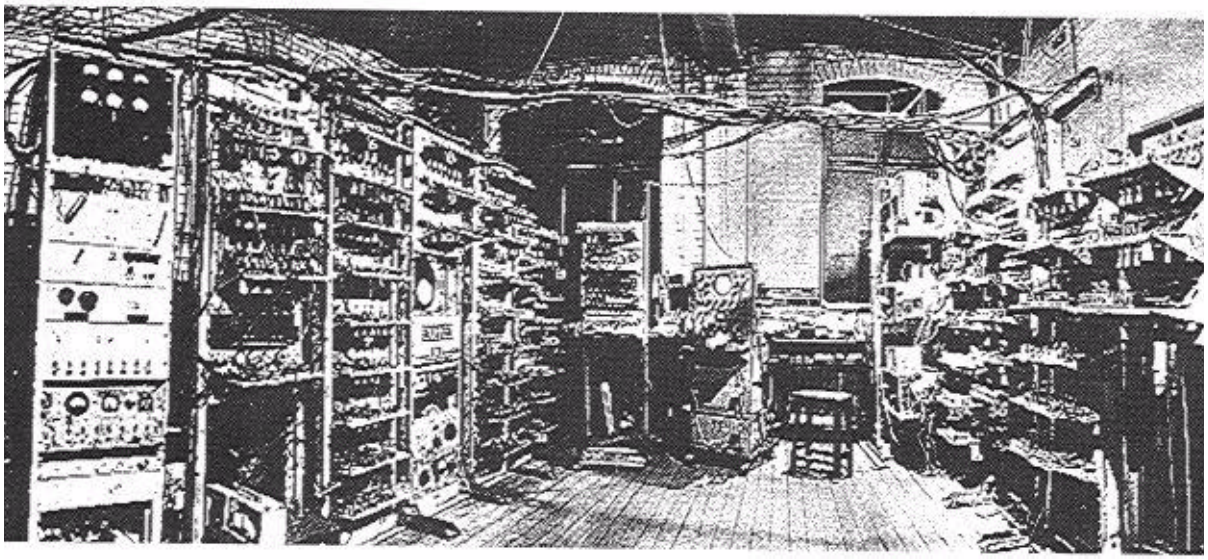
Harvard computer

A stored program computer in which separate memory is employed to hold the program and the data.

Present day computers are von Neuman although usual to have separate cache memories near processor for program and data.

Slide 19

The world's first electronic *stored program* computer



The Manchester University Mark I, operational June 21, 1948

Slide 20

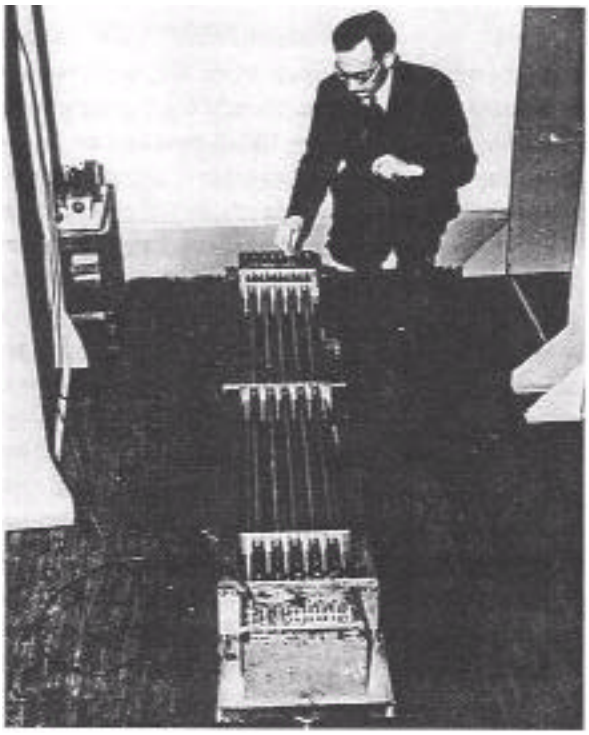
EDSAC

Electronic Delay Storage Automatic Calculator

Operational in 1949 - first large scale stored program computer.

Cambridge University

Used mercury delay line memory



Maurice Wilkes looking at the delay lines.

Stretch Computer

1961 IBM - Designed to "stretch" technology/performance to its limits - germanium transistor based - much faster than earlier tube based systems (IBM 704/5.) e.g. 1 microsecond add compared to 84 microsecond add.

Landmarks in Computer Design since 1960

Supercomputers

Mid 1960's - CDC 6600 - one of the first supercomputers, multiple functional units, classic 3-address instruction format (re-introduced in RISC computers in 1990's), refrigerated. Follow-on CDC 7600.

1970's, early 1980's supercomputers continue to be deveoped. Cray 1 and Cray 2 supercomputers using the most advanced technology available to obtain the maximum speed.

Slide 23

Development of families

Processors developed in "families" such that processors would be able to execute programs of earlier processors. Started with IBM 360 series in 1960's.

Concept used by all manufacturers.

Slide 24

1970's - minicomputers appeared - much lower performance but low cost and bringing computers to the laboratory - PDP 8 being the classic.

First microprocessors appeared using MOS technology (4004). Intel family starts.

Early 1980's Introduction of the personal computer (PC).

Slide 25

Microprocessor families

Eight-bit microprocessors, that is, processors that can operate upon and perform arithmetic on 8-bit numbers directly, in the mid- 1970s, typified by the Intel 8080, Motorola MC6800 and Zilog Z-80.

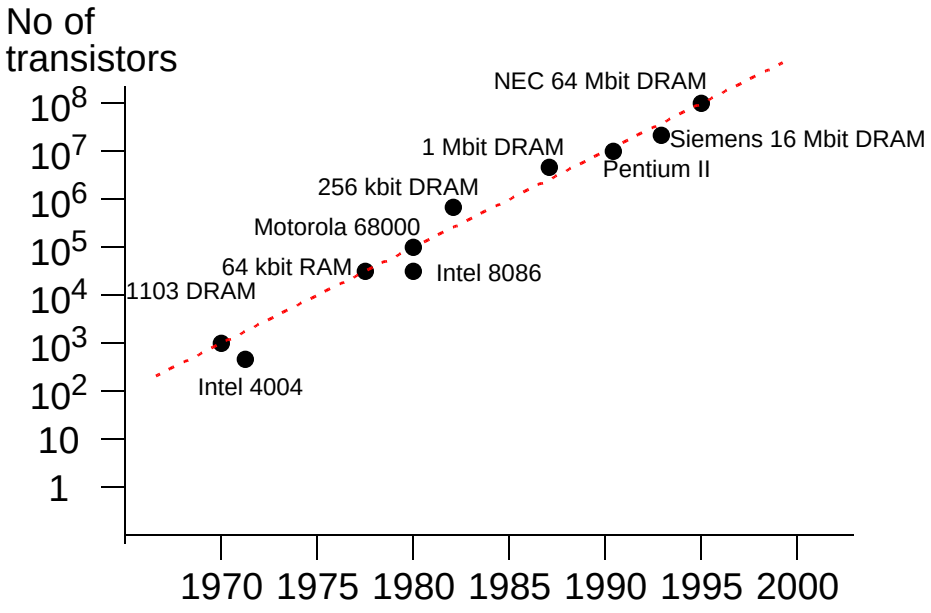
Sixteen-bit microprocessors towards the end of the 1970s, e.g., Intel 8086 and Motorola MC68000, both introduced in 1978.

Thirty-two bit processors appeared in 1980s (e.g., Intel 386, Motorola MC68020, and MC68030. Intel 486 and Motorola MC68040 continued the trend of adding facilities within the chip (floating point units).

Slide 26

1980's - Dominated by increasing integrated circuit performance.

Moores law (1965)- number of transistors on a chip doubles every year (or more acurately quadruples every three years, or 59%/year). Still applies today:



Development of microprocessor families cont.

Superscalar processors in early 1990s - more than one instruction can be executed in each cycle, e.g. Intel Pentium and Pentium Pro. Pentium II introduced in 1996, extra instructions for multimedia applications (MMX technology). Pentium III, Pentium IV, ...

Sixty-four bit processors in mid 1990s.

Also Intel pursuing a design in which instructions are packaged into groups for simultaneous execution (see much later).

Reduced Instruction Set Computer (RISC)

RISC emerged in early 1980s. Instruction set carefully chosen (perhaps less than 100 instructions) and a few addressing modes (perhaps 2–5) – leads to processor that can operate faster - now basis of all processors internally.

Present (2001)

Still dominated by increasing integrated circuit performance and increasing clock speeds

Intel family still dominates the home market with increasing complex backward compatible processors

Workstations - based upon RISC processors (most notably SUNs) higher performance

By the end of the 1990's, both RISC and Intel processors still competing.