King Fahd University of Petroleum and Minerals
Department of Computer Engineering

COMPUTER ARCHITECTURE COE 308

Homework 4

To be submitted on 26 December 2012

Problems	Grading
1	
2	
3	
TOTAL	

Question-1: Principles of Hierarchical Memory

The idea of caching code and data is based upon the principle of locality. Give a (1) short definition and (2) one example for each type of locality:

a. Give a short definition and an example of temporal data locality

b. Give a short definition and an example of temporal code locality

c. Give a short definition and an example of spatial data locality

d. Give a short definition and an example of spatial code locality

Question-2: Hierarchical Memory Systems

A computer has a processor P with a hierarchical memory system that consists of a 4-ways set-associative cache memory CM and a main-memory MM. P generates a 32-bit memory address ADDR = (TAG, Index, Word). CM has 64-entries. The page size is 32 bytes, where each word addressed by P is one byte. MM has Tmm=18 ns access time. Denote by (Tcm) and (Ph) as CM access time and its hit probability, respectively.

Answer each of the following questions:

1. Find the number of bits in "Index", "Word", and "TAG".
2. Determine the page size in bits.
3. Determine the cache capacity in bits.
4. Determine the main memory capacity in bits.
5. CM can be designed in the following ways: (1) as a 4-way set-associative cache with Tcm = 1.25 ns and Ph = 0.88, (2) as a fully-associative cache with Tcm = 1.5 ns and Ph = 0.97, (3) as a direct-mapped cache with Tcm = 1 ns and Ph = 0.80. Answer each of the above questions:
    a. Which of the above three cache designs has the least conflict misses.
    b. For what reason the direct-mapped cache has the least access time.
    c. For what reason the cache with largest hit probability has the largest access time.
    d. Determine which of the above three cache designs gives the best global performance of hierarchical memory system including CM and MM.

6. The processor is running a benchmark with the following instruction distribution: (1) 55% of R-type, (2) 18% are loads, (3) 12% are stores, and (4) 15% are branching instructions. Suppose the retained cache solution is as a 4-way set-associative cache with Tcm = 1.25 ns and Ph = 0.8 which is used as an instruction cache and as a data cache. Answer each of the following questions:
    a. Evaluate the average access time of the memory.
    b. Evaluate the average stall time per instruction (Tstall).
    c. Evaluate the CPI for this processor if the ideal CPI is 2 clocks and processor clock rate is 1 GHz.

Question-3: SHARED-MEMORY MULTIPROCESSORS

1. Consider the MIMD family of multiprocessors. Shortly describe how inter-processor communication works in a (1) Shared-Memory Multiprocessor, and (2) Distributed-Memory Multi-computer.

2. Jacobi Synchronous Iteration example consists of iteratively solving a linear system equation which consists of n linear equations with n unknowns:

$$
\begin{aligned}
a_{n-1,0}\,x_0 + a_{n-1,1}x_1 + a_{n-1,2}\,x_2 \ldots + a_{n-1,n-1}x_{n-1} &= b_{n-1} \\
&\vdots \\
a_{1,0}\,x_0 + a_{1,1}\,x_1 + a_{1,2}x_2 \ldots + a_{1,n-1}x_{n-1} &= b_1 \\
a_{0,0}\,x_0 + a_{0,1}x_1 + a_{0,2}\,x_2 \ldots + a_{0,n-1}\,x_{n-1} &= b_0
\end{aligned}
$$

   In the kth iteration, Jacobi iteratively solving the above systems consists of rearranging the ith equation as follows:

$$a_{i,0}\,x_0 + a_{i,1}x_1 + a_{i,2}\,x_2 \ldots + a_{i,n-1}\,x_{n-1} = b_i$$

   and write the solution x_i out of the ith equation

$$x_i = (1/a_{i,i})[b_i - (a_{i,0}\,x_0 + a_{i,1}x_1 + a_{i,2}\,x_2 \ldots a_{i,i-1}\,x_{i-1} + a_{i,i+1}\,x_{i+1} + a_{i,n-1}\,x_{n-1})]$$

or

   Possible initial value of $x_i = b_i$. The solution equation can be used as an iteration formula for each of the unknowns to obtain a better approximation. The Jacobi Iteration consists of updating all the values of x at once in parallel and iterate the process for MaxIter iterations. Note that updated values of x in a given iteration should not be used in the same iteration. We assume n=4096 and MaxIter = 20.

Answer the following questions:

1. Determine the time complexity of a sequential Jacobi Solver with your justifications.

2. Write a sequential code for Jacobi Solver with your short description.

3. Convert the sequential Jacobi Solver into a shared-memory parallel program using the Directive-Based programming (OpenMp pragmas). Run the program over the IBM 1350 Cluster Computer and collect the execution time for one node by varying the number of threads: 1 core, 2 cores, 4 cores, and 8 cores. Evaluate the Speedup for each of the above cases. Plot the speedup for the above program over all the studied cases.