



**King Fahd University of Petroleum and Minerals  
Department of Computer Engineering**

DIGITAL LOGIC DESIGN COE 202

Homework 4, January 13, 2009

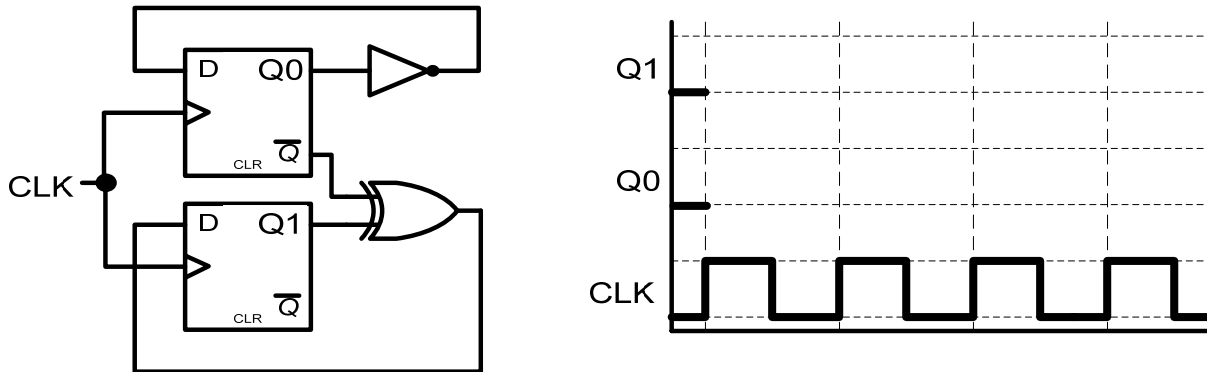
To be returned on January 28, 2009

<b>Problems</b>	<b>Grading</b>
1	
2	
3	
4	
<b>TOTAL</b>	

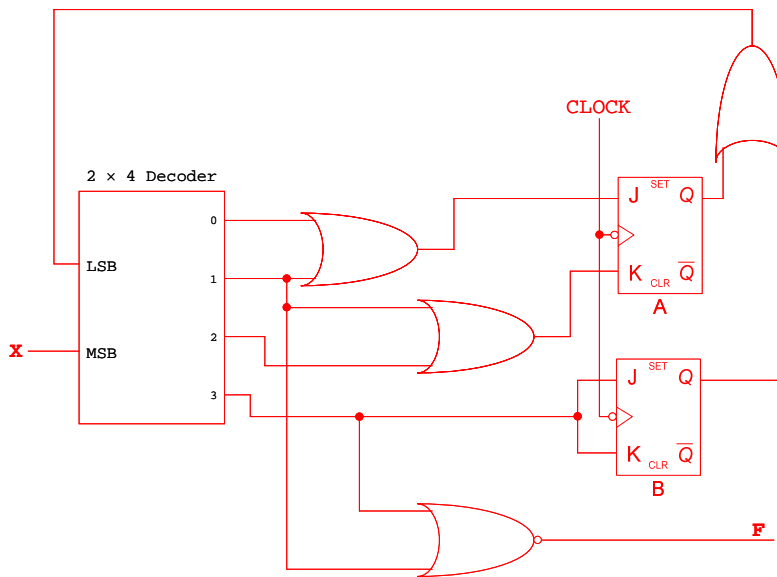
**Student Name:**.....

**Student ID:**.....

**Problem # 1:** Two positive edge-triggered D flip-flops are connected as shown in the figure. Both flip-flops are initialized to 0 at the beginning. Fill in the timing diagram for the two outputs Q1 and Q0.



**Problem # 2:** Drive the state diagram for the following circuit (show all the steps of your work):



**Problem # 3:** Design a *Mealy* sequential circuit that receives data serially on input X and produces an output Y. The output Y is equal to 1 when **all** of the following three conditions are satisfied:

1. The input sequence “10” is detected at least once.
2. At least one “1” is received since the sequence “10” was detected.
3. The total number of “1”s received so far is *odd*.

Use rising-edge triggered *JK* flip-flop(s) and a non-inverted decoder to design the circuit. **Show all steps of the design including state minimization.** The following are sample traces to help you in the design of the state diagram as well as verifying your final design:

1. Trace 1:      $X = 001011110011\dots$   
                   $Y = 000001011101\dots$

2. Trace 2:      $X = 001100011110011\dots$   
                   $Y = 000000010100010\dots$