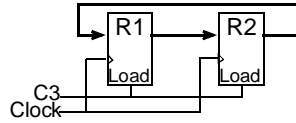


**Problem Solutions to Problems Marked With a * in
Logic Computer Design Fundamentals, Ed. 2**

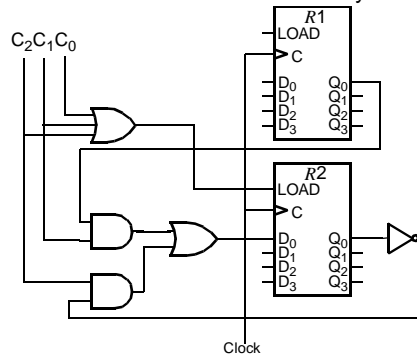
CHAPTER 7

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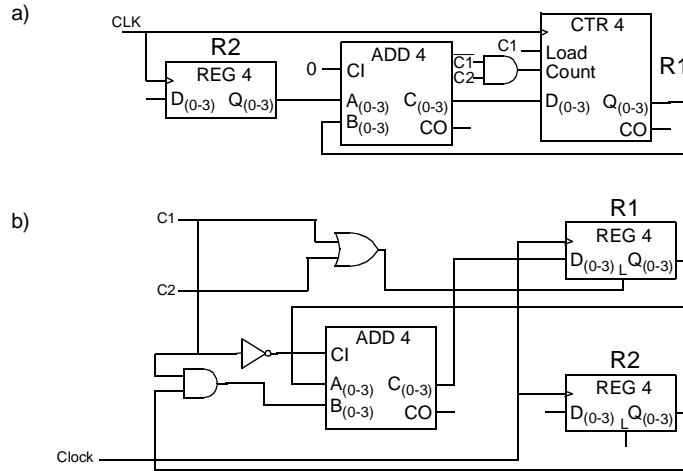
7-1.



7-3. Errata: Interchange statements “Transfer R1 to R2” and “Clear R2 synchronously with the clock.”



7-6.



7-9.

0101 1110	
<u>1100 0101</u>	
0100 0100	AND
1101 1111	OR
1001 1011	XOR

Problem Solutions – Chapter 7

7-11.

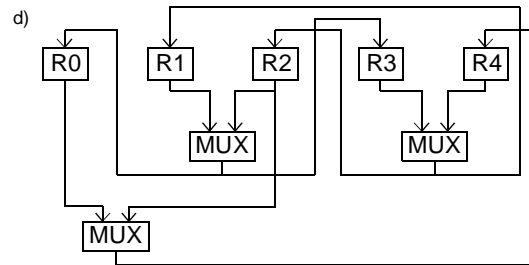
sl 1001 1010

sr 0010 0110

7-14.

- | | |
|------------------------------------|------------------------------------|
| a) Destination <- Source Registers | b) Source Registers -> Destination |
| R0 <- R1, R2 | R0 -> R4 |
| R1 <- R4 | R1 -> R0, R3 |
| R2 <- R3, R4 | R2 -> R0, R4 |
| R3 <- R1 | R3 -> R2 |
| R4 <- R0, R2 | R4 -> R1, R2 |

c) The minimum number of buses needed for operation of the transfers is three since transfer Cb requires three different sources.



7-19.

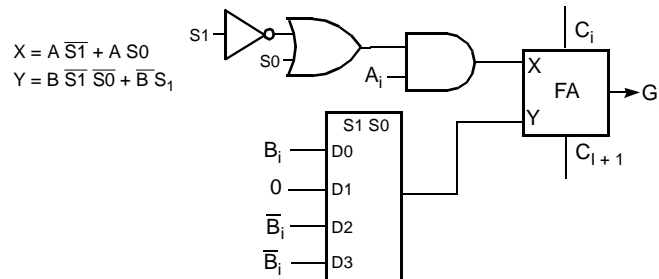
$$C = C_8$$

$$V = C_8 \oplus C_7$$

$$Z = F_7 + F_6 + F_5 + F_4 + F_3 + F_2 + F_1 + F_0$$

$$N = F_7$$

7-22.



7-24.

- a) XOR = 00, NAND = 01, NOR = 10 XNOR = 11
- $$\text{Out} = S_1 \bar{A} \bar{B} + S_0 \bar{A} \bar{B} + \bar{S}_1 \bar{A} B + S_0 A B + \bar{S}_1 S_0 A \bar{B}$$
- b) The above is a simplest result.

7-26.

- (a) 1011 (b) 1010 (c) 0001 (d) 1100

Problem Solutions – Chapter 7

7-28.

- | | |
|---|--|
| <p>(a) $R5 \leftarrow R4 \wedge \overline{R5}$ R5 = 0000 0100</p> <p>(b) $R6 \leftarrow R2 + \overline{R4} + 1$ R6 = 1111 1110</p> <p>(c) $R5 \leftarrow srR0$ R5 = 0000 0000</p> | <p>(d) $R5 \leftarrow DataIn$ R5 = 0001 0010</p> <p>(e) $R4 \leftarrow R4 \oplus Constant$ R4 = 0001 0101</p> <p>(f) $R3 \leftarrow R0 \oplus R0$ R3 = 0000 0000</p> |
|---|--|

7-31.

Clock	AA	BA	MB	OF/EX:A	OF/EX:B	FS	EX/WB:F	EX/WB:DI	MD	RW	DA	R[DA]
1	2	3	0	—	—	—	—	—	—	—	—	—
2	0	6	0	02	03	5	—	—	—	—	—	—
3	7	0	0	00	06	18	FF	—	0	1	1	—
4	0	0	1	07	00	01	0C	—	0	1	4	FF
5	0	3	0	00	02	02	08	—	0	1	7	0C
6	0	0	0	00	03	00	02	—	0	1	1	08
7	0	0	0	00	00	00	00	—	0	0	0	02
8	—	—	—	00	00	0C	00	Data	1	1	4	—
9	—	—	—	—	—	—	00	—	0	1	5	Data
10	—	—	—	—	—	—	—	—	—	—	—	00

The contents of registers that change for a given clock cycle are shown in the next clock cycle. Values are given in hexadecimal.