COE 203 COURSE SYLLABUS

1. **Department, Number and Course Title**

   Department: Computer Engineering
   Course Number: COE 203
   Course Title: Digital Logic Laboratory

2. **Design:** Required Course

3. **Catalog Description**

   Review of Digital Logic Design: Design of Combinational Circuits, and Design of Sequential Circuits. Logic implementation using discrete logic components (TTL, CMOS), and programmable logic devices. Introduction to Field Programmable Logic Arrays (FPGAs). The basic design flow: design capture (schematic capture, HDL design entry, design verification and test, implementation (including some of its practical aspects), and debugging. Design of data path and control unit.

4. **Prerequisite(s)**

   Fundamentals of Computer Engineering (COE 202)

5. **Textbook(s) and/or other Required Material**

   Morris Mano and Charles Kime, Logic and Computer Design Fundamentals, Third Edition, Prentice Hall International, 2004.

6. **Course Objectives**

   After successfully completing the course, students will be able to:
   - Design combinational and sequential circuits using discrete components, EEPROMs, and FPGAs to meet certain specifications.
   - Use basic structural Hardware Description Languages to implement digital circuits.
   - Design and conduct experiments related to digital systems and to analyze their outcomes.

7. **Topics Covered**

I. Combinational Logic Design Review 1 week

- Course Introduction.
- Introduction to Combinational and Sequential Circuits.
- K-maps, universal gates, MSI components, with an example for each.
- Reading assignment on Sequential circuits.
- Assignment 1: Example problem for the covered topics.

II. Sequential Logic Design Review 1 week

- Flip-flops
- Sequential circuits design procedure
- Sequential circuits analysis procedure
- Counters and Registers
- Assignment 2: Review Combinational and Sequential Circuits for next week's quiz.

QUIZ # 1 (Week 3)

III. Prototyping of logic circuits

a. Discrete components (Experiment 1) 1 week

- Introduction to ICs, logic families, 74xx and 54xx
- Power and ground
- Physical implementation of combinational circuits using discrete components
- Implementation of a simple combinational circuit using ICs.

b. EEPROM (Experiment 2) 1 week

- Introduction to logic prototyping using PLDs.
- Implementation of a sequential circuit using EEPROMs and external registers.

c. FPGAs (Experiment 3)

- Introduction to FPGAs design flow 1 week

QUIZ # 2 (Week 6)

- Design and implementation of a sequential circuit using schematic design entry (**Experiment 4)** 1 week
- Introduction to hardware description languages (HDL) **(Experiment 5)** 1 week
  - Structural modeling using verilog
  - Complete design and implementation of a small combinational circuit
- Register Transfer Level (RTL) modeling using verilog **(Experiment 6)** 1 week
  - Complete design and implementation of a simple datapath
- Sequential circuit implementation using verilog **(Experiment 7)** 1 week

QUIZ # 3 (Week 10)

IV. Design and implementation of a data path and control unit (Experiment 8) 2 weeks

- A small processor implementation
  - Large data path and a control unit
  - Integrating HDL and schematic units

V. Project 3 weeks

8. **Class/Laboratory Schedule**

   3 hours per week.

9. **Course Contribution to Meet the Professional Component**

   This course emphasizes the use of FPGAs to implement combinational and sequential circuits. The students use various software tools to model, simulate and implement digital circuits. They also design test benches to analyze certain parameters of the circuits. Every week they are required to submit a lab report of the previous experiment. The course project is intended to build the students' ability to design, implement, simulate, and verify the operation of a simple datapath and control unit. In the project, the students work in teams. At the end they deliver a presentation and submit a project report.

10. **Relationship to Program Outcomes**

    This course supports the following five program outcomes out of the outcomes required by ABET Criterion 3 for accrediting computer engineering programs.

    Outcome 1: The ability to design combinational and sequential circuits to meet certain specifications **[ABET Criterion 3c]**

    Outcome 2: The ability to use tools and discrete components, EEPROMs, FPGAs, to model, simulate and implement digital circuits. **[ABET Criterion 3k]**

    Outcome 3: The ability to design and conduct experiments related to digital systems and to analyze their outcomes. [**ABET Criterion 3b**]

Outcome 4: The ability to work in teams. [**ABET Criterion 3d**]

Outcome 5: The ability to communicate effectively. [**ABET Criterion 3g**]

Grade Distribution:

Experiments (8)	**65%**
Quizzes (3)	**15%**
Project	**20%**

Lab. Reports:
Pre-Lab reports should be submitted at the beginning of the lab.
Lab. Reports should be submitted before the next lab session.

Attendance:

- Regular attendance is a university requirement. Attendance will be taken at the beginning of every class.
- Whenever the number of unexcused absences exceeds **20%** of the held classes, the grade DN will be reported without any formal warning as per the university rule.
- In case of an absence, a make up can be arranged provided that:
    1. The student has an official excuse.
    2. Both the student lab instructor and the instructor of the section in which the student is making up his lab mutually agree on the make up.
    3. The mark for that lab is sent by the instructor with whom the student made up the lab with.

- In case of late attendance, 10% marks will be deducted from that lab.

General Notes:

- Cheating is not allowed. Severe measures will be taken by the instructor.
- Any use of the **internet** during class/lab time is **prohibited and results in zero score** in the lab work.
- Mobile phones **must** be turned off or made silent during the class/lab session.

Class Discussion
Participation in class discussion is very much encouraged. Asking questions during the labs helps both the instructor and the student. The instructor gets the feedback and the students get the point clarified.

Grading Issues
All the grading issues must be resolved within a week after the return of graded material.

Instructor

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