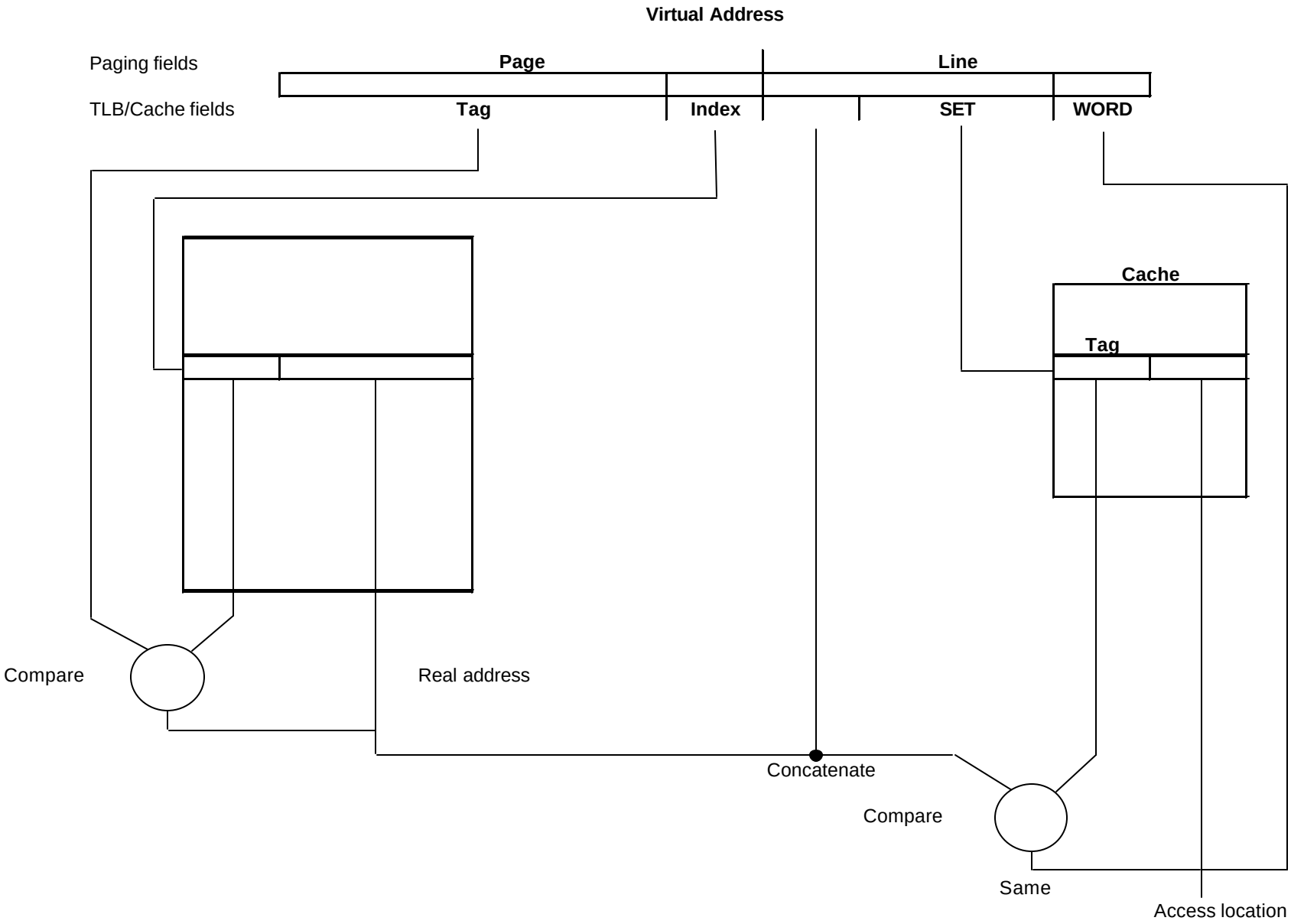
Virtual Address
Paging fields
Page
Line
TLB/Cache fields
Tag
Index
SET
WORD
Cache
Tag
Compare
Real address
Concatenate
Compare
Same
Access location

- To find the "Line" field, each page size is 16 KBytes = 2^{14} ⇒ "Line" bits = 14 bits
- To find the "Page" field, there are (2^{40} / 16 Kbytes) = 2^{26} pages (where 40 is the size of the virtual address) ⇒ "Page " bits = 26 bits
- To find the TLB "Index" field, the TLB has 256 entries with 2-way set associative mapping, i.e. 256 / 2 = 128 sets ⇒ TLB "Index" bits = 7 bits
- To find the TLB "Tag" field, the "Page" field is 26 bits wide and the "Index" field is 7 bits wide ⇒ TLB "Tag" bits = 19 bits
- To find the "WORD" field, each block of cache consists of 32-bits or 4 words ⇒ "WORD" bits = 2 bits
- To find the "SET" field, the cache has 1024 blocks with 4-way set associative mapping, i.e. 1024 / 4 = 256 sets ⇒ "SET" bits = 8 bits
- To find the cache "TAG" field, there are 2^{32} / 4 = 2^{30} MM blocks mapped to 256 cache sets ⇒ cache "TAG" bits = $\log_2$ (2^{30} / 256 sets) = 22 bits

Note that there are 4 bits ("Line" bits – "SET" bits – "WORD" bits = 14 – 8 – 2 = 4 bits) that will be concatenated with the data provided by the TLB. The resultant will be compared with the "TAG" field stored in cache. Thus, the data provided by the TLB is (22 bits – 4 bits) = 18 bits wide = bits needed to represent MM pages (i.e. (2^{32} / 16 Kbytes) = 2^{18} pages (where 32 is the size of the real address) ⇒ MM "Page " bits = 18 bits).