Microinstruction Format and Decode

μ-instruction format	Dest	ALU	Src1	Src2	Constant	Misc	Cond	Jump Addr
0000	None	None	None		None	None	None	
0001	C	ADD	A		4	MDR ← M[MAR]	Uncond	
0010	PC	SUB		B		M[MAR] ← MDR	zero?	
0011	MAR	RR	PC			A ← Rs1	negative?	
0100	MDR	RL	MAR			B ← Rs2	carry?	
0101	IR	SR	MDR			B ← Rd	overflow?	
0110		SL	IR (16 bits)			Rd ← C	Decode	
0111		AND	IR (26 bits)			R31 ← C		
1000		OR	Constant					
1001		XOR						
1010		NOT						
1011		Pass S1						
1100		Pass S2						
1101								
1110								
1111								

Opcode	Absolute Addr	Label
LD	5	**Load:**
ST	8	**Store:**
BEQ	12	**BEQ:**
BNE	14	**BNE:**
BL	16	**BL:**
BGE	18	**BGE:**
JAL	20	**JAL:**
J (PC relative)	22	**JPC:**
J (Register indirect)	23	**JR:**
ADD (R-R-R)	24	**ADDR:**
SUB (R-R-R)	25	**SUBR:**
RR (R-R-R)	26	**RRR:**
RL (R-R-R)	27	**RLR:**
SR (R-R-R)	28	**SRR:**
SL (R-R-R)	29	**SLR:**
AND (R-R-R)	30	**ANDR:**
OR (R-R-R)	31	**ORR:**
XOR (R-R-R)	32	**XORR:**
NOT (R-R-R)	33	**NOTR:**
ADD (R-R-I)	34	**ADDI:**
SUB (R-R-I)	35	**SUBI:**
RR (R-R-I)	36	**RRI:**
RL (R-R-I)	37	**RLI:**
SR (R-R-I)	38	**SRI:**
SL (R-R-I)	39	**SLI:**
AND (R-R-I)	40	**ANDI:**
OR (R-R-I)	41	**ORI:**
XOR (R-R-I)	42	**XORI:**
NOT (R-R-I)	43	**NOTI:**

Microprograms

Loc	Label	Dest	ALU	Src1	Src2	Constant	Misc	Cond	Jump Addr
0	**Ifetch:**	MAR	Pass S1	PC	None	None	None	None	
1		None	None	None	None	None	MDR ← M[MAR]	None	
2		IR	Pass S1	MDR	None	None	None	None	
3		PC	ADD	PC	Constant	4	A ← Rs1	None	
4		None	None	None	None	None	B ← Rs2	Decode	
5	**Load:**	MAR	ADD	A	IR (16 bits)	None	None	None	
6		None	None	None	None	None	MDR ← M[MAR]	None	
7		C	Pass S1	MDR	None	None	None	Uncond	**Write:**
8	**Store:**	None	None	None	None	None	B ← Rd	None	
9		MAR	ADD	A	IR (16 bits)	None	None	None	
10		MDR	Pass S2	None	B	None	None	None	
11		None	None	None	None	None	M[MAR] ← MDR	Uncond	**Ifetch:**
12	**BEQ:**	None	SUB	A	B	None	None	zero?	**Branch:**
13		None	None	None	None	None	None	Uncond	**Ifetch:**
14	**BNE:**	None	SUB	A	B	None	None	zero?	**Ifetch:**
15		None	None	None	None	None	None	Uncond	**Branch:**
16	**BL:**	None	SUB	A	B	None	None	negative?	**Branch:**
17		None	None	None	None	None	None	Uncond	**Ifetch:**
18	**BGE:**	None	SUB	A	B	None	None	negative?	**Ifetch:**
19	**Branch:**	PC	ADD	PC	IR (16 bits)	None	None	Uncond	**Ifetch:**
20	**JAL:**	C	Pass S1	PC	None	None	None	None	
21		None	None	None	None	None	R31 ← C	None	
22	**JPC:**	PC	ADD	PC	IR (26 bits)	None	None	Uncond	**Ifetch:**
23	**JR:**	PC	ADD	A	IR (16 bits)	None	None	Uncond	**Ifetch:**
24	**ADDR:**	C	ADD	A	B	None	None	Uncond	**Write:**
25	**SUBR:**	C	SUB	A	B	None	None	Uncond	**Write:**
26	**RRR:**	C	RR	A	B	None	None	Uncond	**Write:**
27	**RLR:**	C	RL	A	B	None	None	Uncond	**Write:**
28	**SRR:**	C	SR	A	B	None	None	Uncond	**Write:**
29	**SLR:**	C	SL	A	B	None	None	Uncond	**Write:**
30	**ANDR:**	C	AND	A	B	None	None	Uncond	**Write:**
31	**ORR:**	C	OR	A	B	None	None	Uncond	**Write:**
32	**XORR:**	C	XOR	A	B	None	None	Uncond	**Write:**
33	**NOTR:**	C	NOT	A	B	None	None	Uncond	**Write:**
34	**ADDI:**	C	ADD	A	IR (16 bits)	None	None	Uncond	**Write:**
35	**SUBI:**	C	SUB	A	IR (16 bits)	None	None	Uncond	**Write:**
36	**RRI:**	C	RR	A	IR (16 bits)	None	None	Uncond	**Write:**
37	**RLI:**	C	RL	A	IR (16 bits)	None	None	Uncond	**Write:**
38	**SRI:**	C	SR	A	IR (16 bits)	None	None	Uncond	**Write:**
39	**SLI:**	C	SL	A	IR (16 bits)	None	None	Uncond	**Write:**
40	**ANDI:**	C	AND	A	IR (16 bits)	None	None	Uncond	**Write:**
41	**ORI:**	C	OR	A	IR (16 bits)	None	None	Uncond	**Write:**
42	**XORI:**	C	XOR	A	IR (16 bits)	None	None	Uncond	**Write:**
43	**NOTI:**	C	NOT	A	IR (16 bits)	None	None	None	
44	**Write:**	None	None	None	None	None	Rd ← C	Uncond	**Ifetch:**