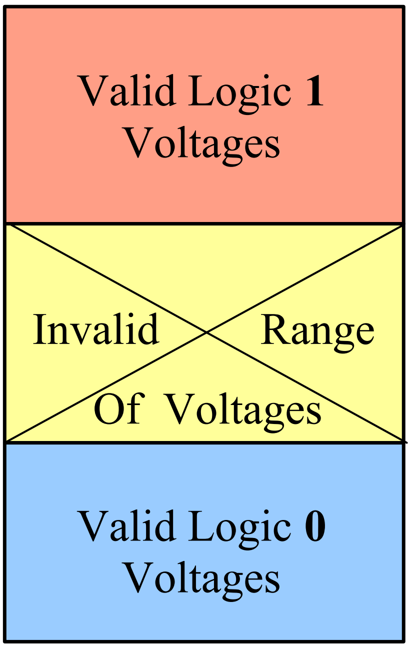
Practical Aspects Of Logic Gates

Introduction & Objectives

- Logic gates are physically implemented as Integrated Circuits (**IC**).
- Integrated circuits are implemented in several technologies.
- Two landmark IC technologies are the **TTL** and the **CMOS** technologies.
- Major physical properties of a digital IC depend on the implementation technology.
- In this lesson, the following major properties of digital IC's are described:
    1. Allowed physical range of voltages for logic 0 and logic 1,
    2. Gate propagation delay/ speed,
    3. The fanin and fanout of a gate,
    4. The use of buffers, and
    5. Tri-State drivers

Allowed Voltage Levels



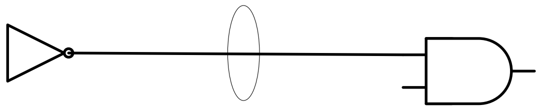
- Practically, logic 0 is represented by a **certain** *RANGE* of Voltages rather than by a single voltage level.
- .In other words, if the voltage level of a signal falls in this range, the signal has a logic 0 value.
- Likewise, logic 1 is represented by a different *RANGE* of **valid** voltages.
- The range of voltages between the highest logic 0 voltage level and the lowest logic 1 voltage level is an "*Illegal Voltage Range*".
- **No signal is allowed to assume a voltage value in this range.**

Input & Output Voltage Ranges

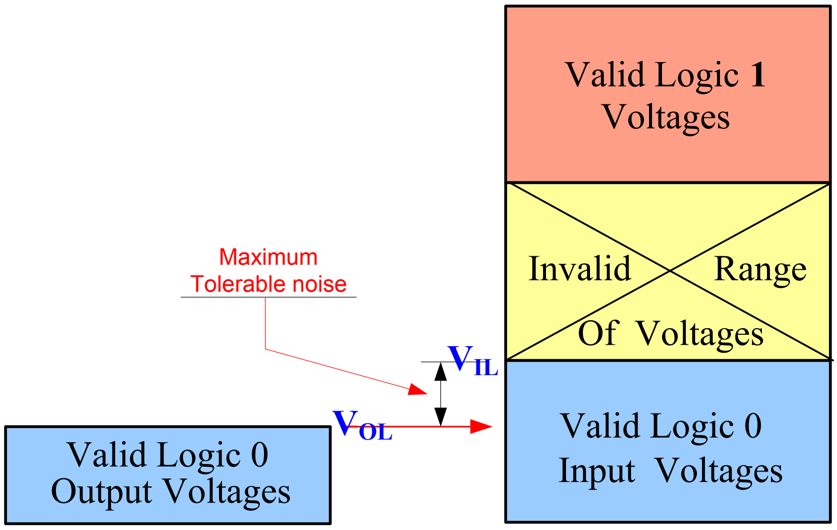
- Inputs and outputs of IC's *do not have the same allowed range of voltages* neither for logic 0 nor for logic 1.
- V_{IL} is the maximum *input* voltage that considered a *Logic 0*.
- V_{OL} is the maximum *output* voltage that considered a *Logic 0*.
- V_{OL} must be lower than V_{IL} to guard against noise disturbance.

Why is $V_{IL} > V_{OL}$?

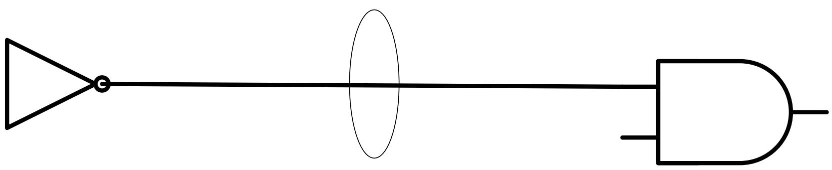
- Consider the case of connecting the output of gate **A** to the input of another gate **B**:



  - The logic 0 output of **A** must be within the range of acceptable logic 0 voltages of gate **B** inputs.
  - Voltage level at the input of **B** = Voltage level at the output of **A** + Noise Voltage
  - If the highest logic 0 output voltage of **A** (V_{OL}) is equal to the highest logic 0 input voltage of **B** (V_{IL}), then the noise signal can cause the actual voltage at the input of **B** to fall in the *invalid range* of voltages.

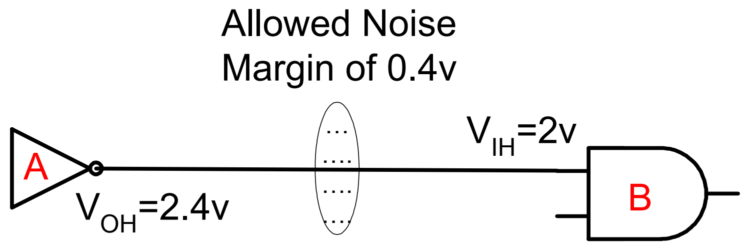


- Accordingly, V_{OL} is designed to be lower than V_{IL} to allow for some noise margin.

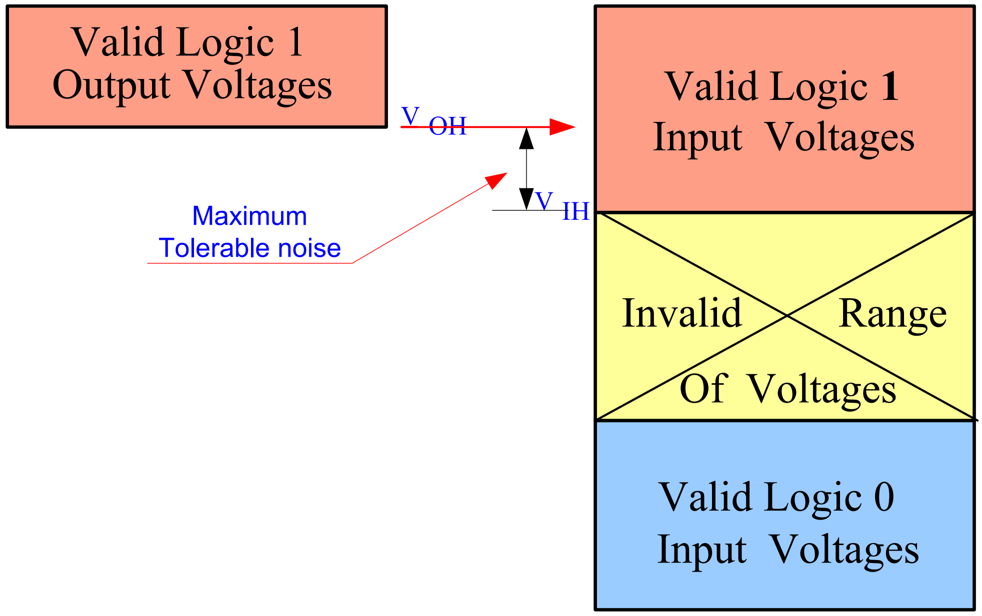


- The difference (V_{IL} - V_{OL}) is thus known as the noise margin for logic 0 (NM_0).
- V_{IH} is the minimum *input* voltage that considered a *Logic 1*.
- V_{OH} is the minimum *output* voltage that considered a *Logic 1*.
- V_{OH} must be higher than V_{IH} to guard against noise signals.

Why is $V_{OH} > V_{IH}$?



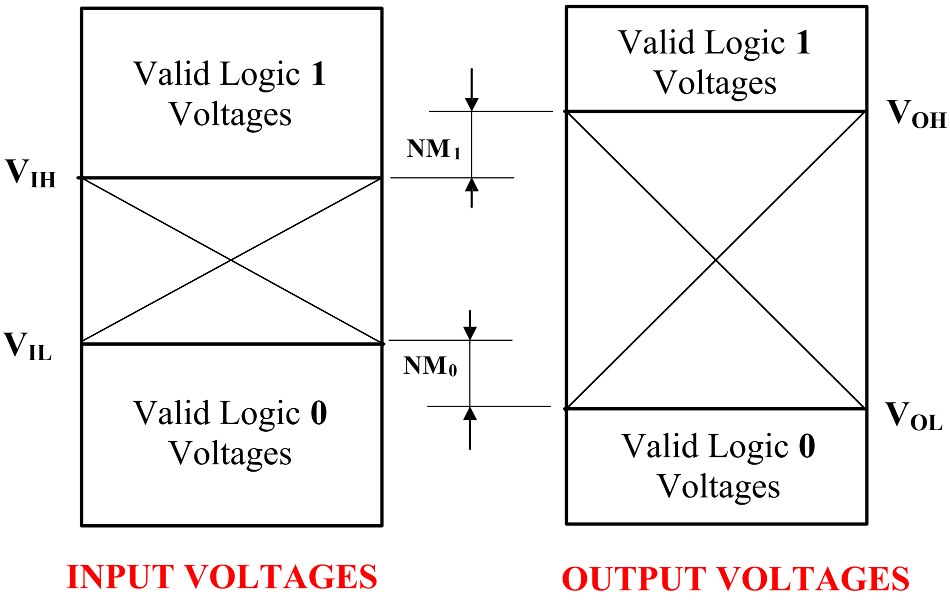
- Consider the case of connecting the output of gate **A** to the input of another gate **B**:
  - The logic 1 output of **A** must accepted as logic 1 by the input of gate **B.**
  - Thus, the logic 1 output of **A** must be *within* the range of voltages which are acceptable as logic 1 input for gate **B**.
  - If the lowest logic 1 output voltage of **A** (V_{OH}) is equal to the lowest logic 1 input voltage of **B** (V_{IH}), then noise signals can cause the actual voltage at the input of **B** to fall in the *invalid range* of input voltages.

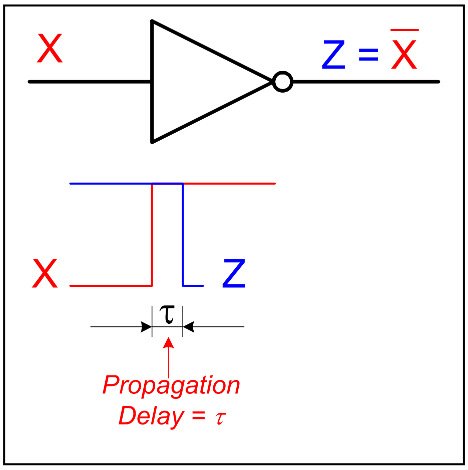


- Accordingly, V_{OH} is designed to be higher than V_{IH} to allow for some noise margin.
- The difference (V_{OH} - V_{IH}) is thus known as the noise margin for logic 1 (NM_1).

Definition

- *Noise margin* is the maximum *noise voltage that can be* added to the input signal of a digital circuit without causing an undesirable change in the circuit output..





Propagation Delay

Consider the shown inverter with input X and output Z.

- A change in the input (X) from 0 to 1 causes the inverter output (Z) to change from 1 to 0.
- The change in the output (Z), however is *not instantaneous*. Rather, it occurs slightly after the input change.
- This *delay* between an input signal change and the corresponding output signal change is what is known as the *propagation delay*.

In general,

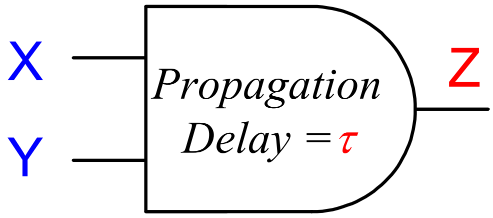
- A signal change on the input of some IC takes a finite amount of time to cause a corresponding change on the output.
- This finite delay time is known as **Propagation Delay**.
- Faster circuits are characterized by smaller propagation delays.
- Higher performance systems require higher speeds (smaller propagation delays).

Timing Diagrams

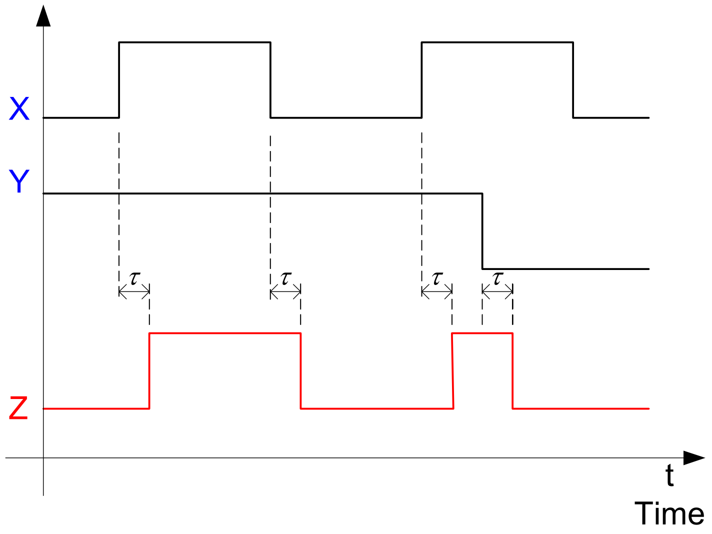
- A timing diagram shows the logic values of signals in a circuit versus time.
- A signal shape versus time is typically referred to as *Waveform*.

Example

The figure shows the timing diagram of a 2-input AND gate. The gate is assumed to have a propagation delay of τ.



- The timing diagram shown Figure illustrates the waveforms of signals X, Y, and Z.
- Note how the output **Z** is delayed from changes of the input signals **X** & **Y** by the amount of the gate **Propagation Delay** τ.

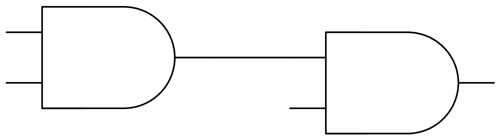


Fanin Limitations

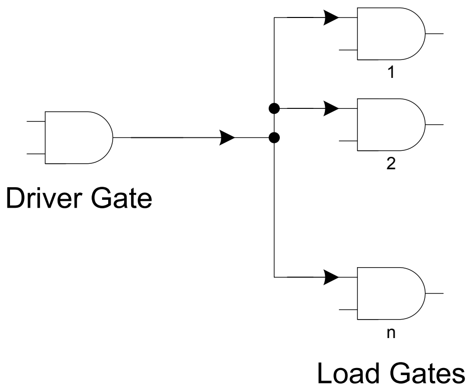
- The *fanin of a* gate is the number of inputs of this gate.
- Thus, a 4-input AND gate is said to have a *fanin* of 4.
- A physical gate cannot have a large number of inputs (*fanin*).

- •For CMOS technology, the more inputs a gate has the slower it is (larger propagation delay). For example, a 4-input AND gate is slower than a 2-input one.
- In CMOS technology, no more than 4-input gates are typically built since more than 4 inputs makes the devices too slow.
- TTL gates can have more inputs (e.g, 8 input NAND 7430).

Fanout Limitations



- If the output of some gate **A** is connected to the input of another gate **B**, gate **A** is said to be *driving* gate, while gate **B** is said to be the *load* gate.
- As the Figure shows, a driver gate may have more than one load gate.



- There is a limit to the number of gate inputs that a single output can drive.
- The *fanout of a* gate is the largest number of gate inputs this gate can drive.
- For TTL, the *fanout* limit is based on CURRENT.
  - A TTL *output* can supply a maximum current $\mathbf{I}_{OL}$ = 16 mA (milliamps)
  - A TTL *input* requires a current of $\mathbf{I}_{IL}$ =1.6mA.
  - Thus, the *fanout* for TTL is 16mA/1.6 mA = 10 loads.
- For CMOS, the limit is based on SPEED/propagation delay.
  - A CMOS input resembles a capacitive load (≈10 pf - picofarads).
  - The more inputs tied to a single output, the higher the capacitive load.
  - The HIGHER the capacitive load, the SLOWER the propagation delay.

- Typically, it is advisable to avoid loads much higher than about 8 loads.

Q. What is meant by the *DRIVE* of a gate?

A. It is the "*CURRENT*" driving-ability of a gate. In other words, it is the amount of current the gate can deliver to its load devices.

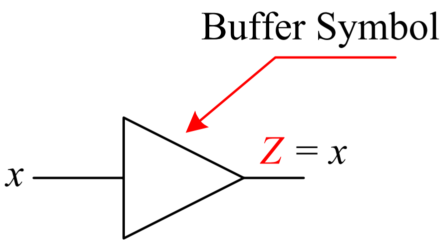
- A gate with *high-drive* is capable of driving more load gates than another with *low-drive*.

Q. How to drive a number of load gates that is larger than the fanout of the driver gate?

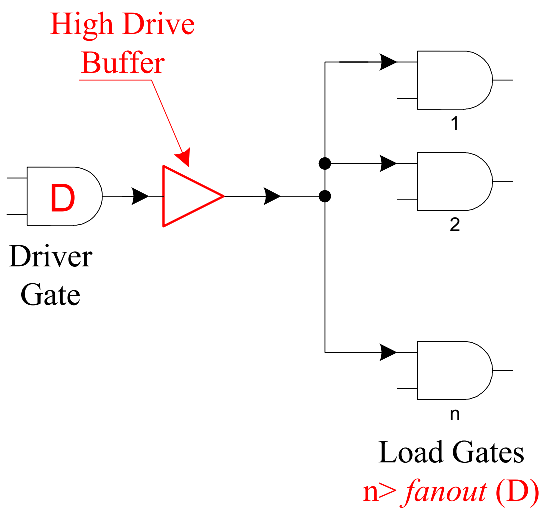
A. In this case, we can use one of two methods:

1. Use high drive buffers
2. Use multiple drivers.

Use of High-Drive Buffers:



- A buffer is a single input, single output gate where the logic value of the output equals that of the input.
- The logic symbol of the buffer is shown in the Figure.
- The buffer provides the necessary drive capability which allows driving larger loads.
- Note that the symbol of the buffer resembles the inverter symbol except that it does not have the inverting circle that the inverter symbol has.
- The figure shows how the buffer is used to drive the large load.

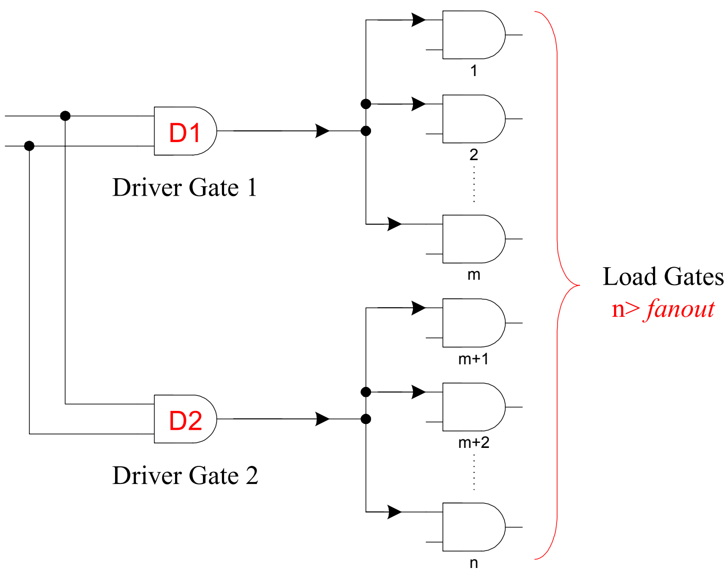


Use of Multiple Drivers:

- The Figure shows the case of 2 identical drivers driving the load gates.
- In general, the large number of load

gates is divided among more than one driver such that each of the identical drivers is driving no more than the fanout.

❖ The multiple driver gates (D1, D2) are of identical type and should be connected to the same input signals



Tri-State Outputs

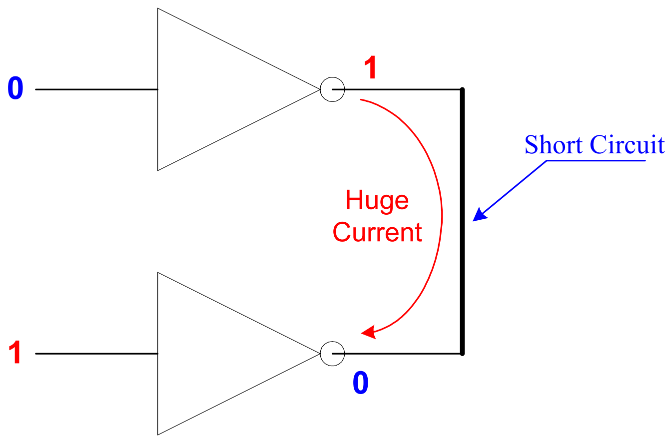
Q. Can the outputs of 2 ICs, or 2 gates, be directly connected?

A. Generally, Nooooooooooo!!! This is only possible if special types of gates are used.

Q. Why cann't the outputs of 2 normal gates be directly connected?

A. Because this causes a ***short Circuit*** that results in huge current flow with a subsequent potential for damaging the circuit.

- This is obvious since one output may be at logic 1 (High voltage), while the other output may be at logic 0 (Low voltage).
- Furthermore, the common voltage level of the shorted outputs will most likely fall in the invalid range of voltage levels.



Q. What are the types of IC output pins that can be directly connected?

A. These are pins/gates with special output drivers. The two main types are:

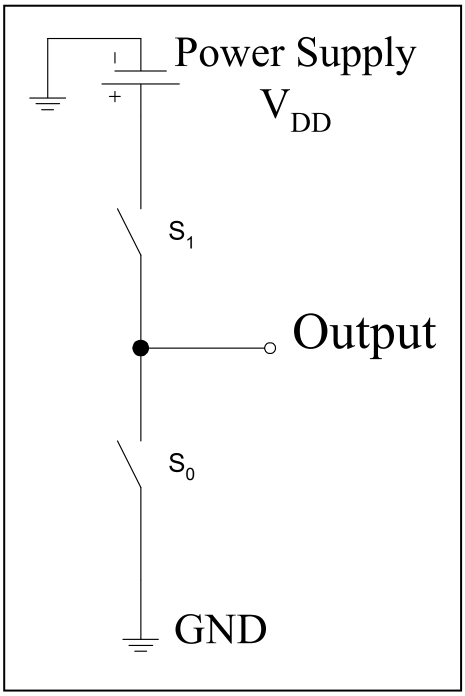
- Open-Collector outputs → this will not be discussed in this course.
- Outputs with Tri-State capability.

Gates with Tri-State Outputs

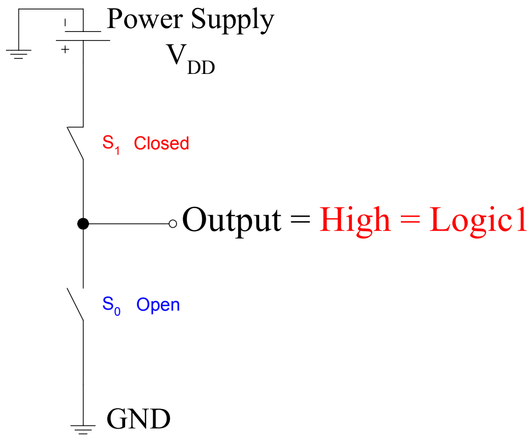
- These gates can be in one of 2 possible states:
    1. An enabled state where the output may assume one of two possible values:
        - Logic 0 value (low voltage)
        - Logic 1 value (high voltage)
    2. A disabled state where the gate output is in a the Hi-impedance (Hi-Z) state. In this case, the gate output is disconnected (open-circuit) from the wire it is driving.
- An enable input (E) is used to control the gate into either the enabled or disabled state.
- The enable input (E) may be either active high or active low.
- Any gate or IC output may be provided with tri-state capability.

Output State Illustrations

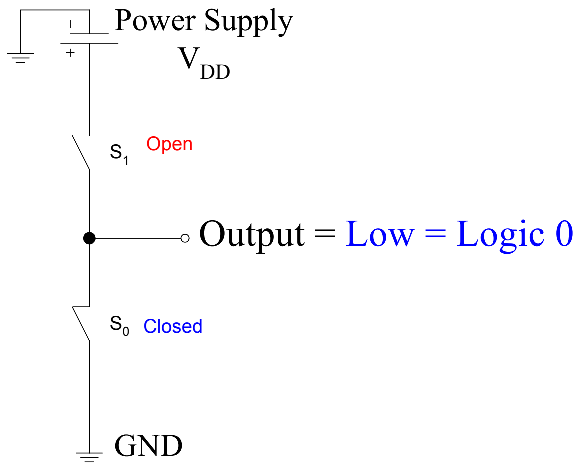
- A generalized output driver can be simply modeled using 2 switches S_1 and S_0 as shown in Figure.
- The output state is defined by the state of the 2 switches (closed -open)
- If S_1 is closed and S_0 is open, the output is high (logic 1) since it is connected to the power supply (V_{DD}).



- If S_1 is open and S_0 is closed, the output is low (logic 0) since it is connected to the ground voltage (0 volt).

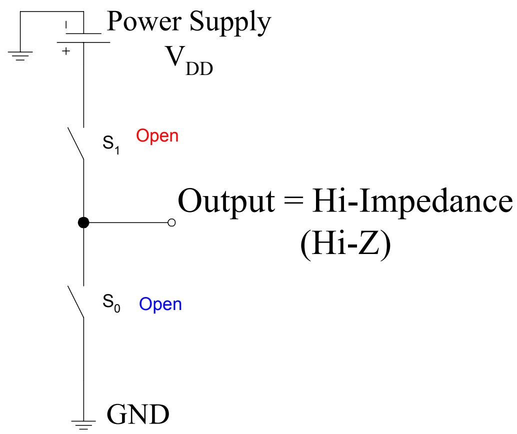


- If, however, both S_1 is and S_0 are open, then the output is neither connected to ground nor to the power supply. In this case, the output node is floating or is in the Hi-Impedance (Hi-Z) state.

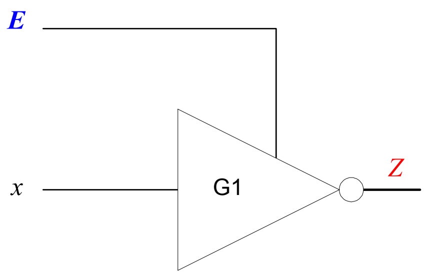


Examples

a) Tri-State Inverter with active high enable



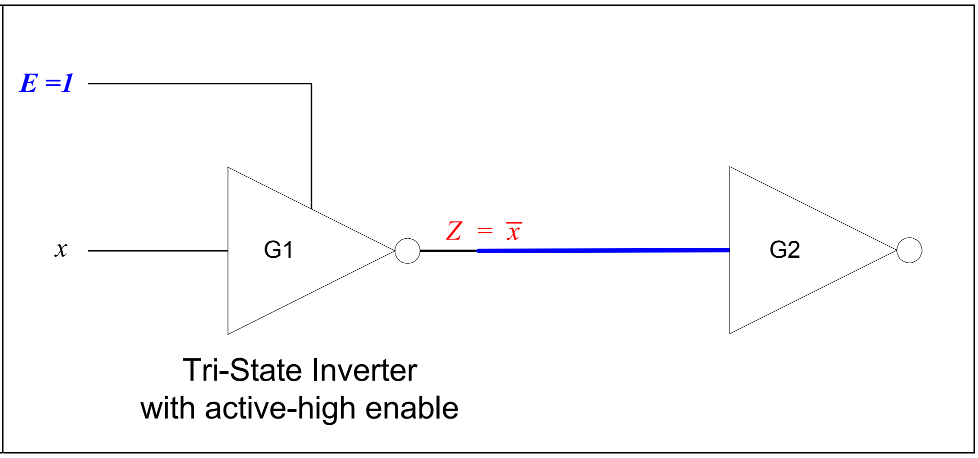
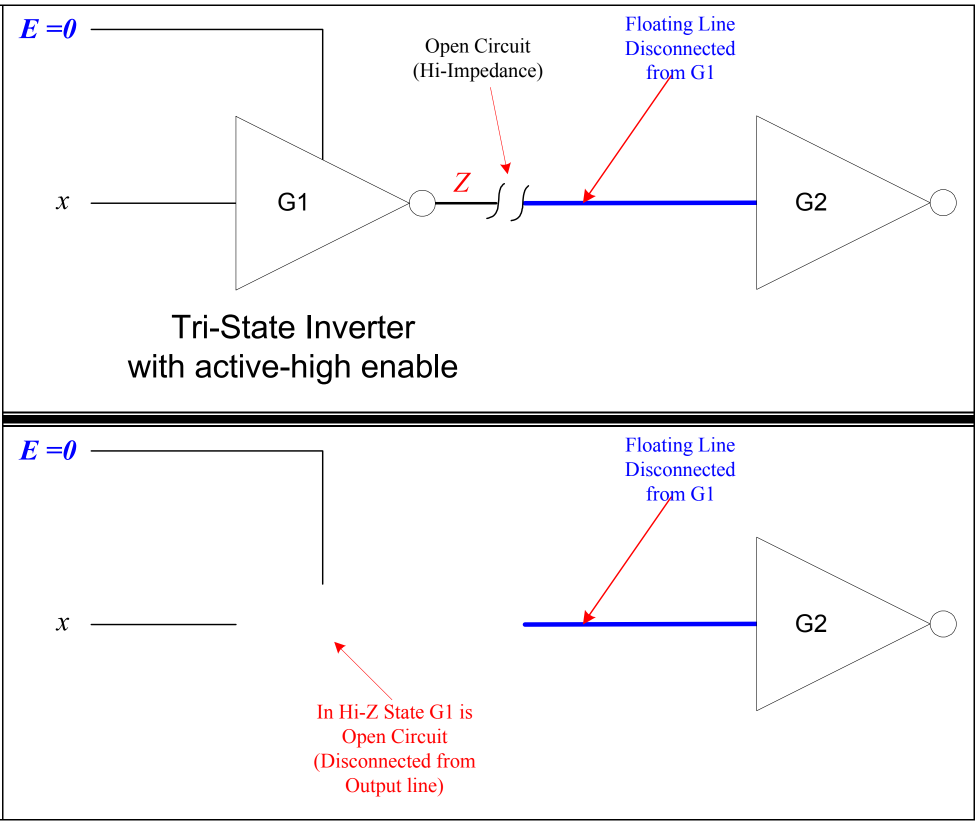
Logic Symbol



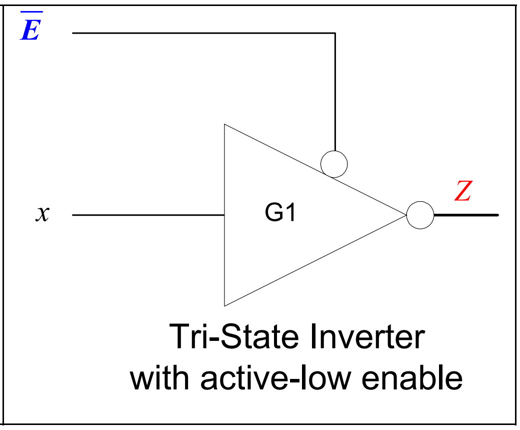
Tri-State Inverter
with active-high enable

Truth Table

E	x	Z
1	0	1
1	1	0
0	0	Hi-Z
0	1	Hi-Z

Enabled State	
Dis-abled State	

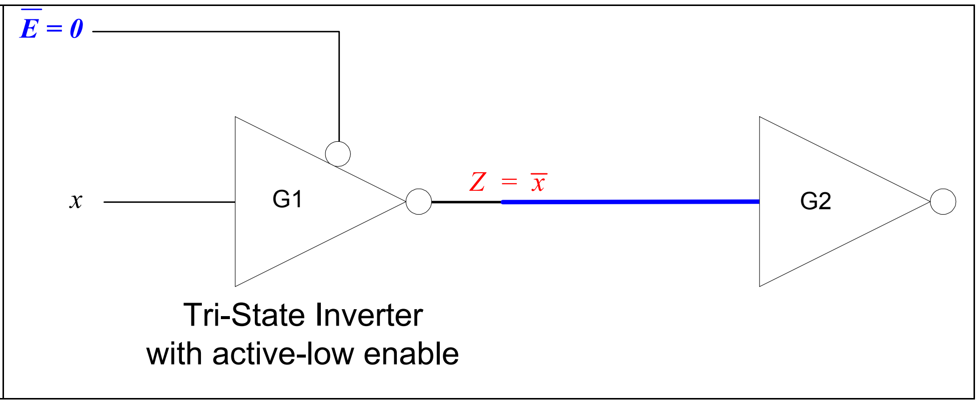
b) Tri-State Inverter with active low enable

Logic Symbol	

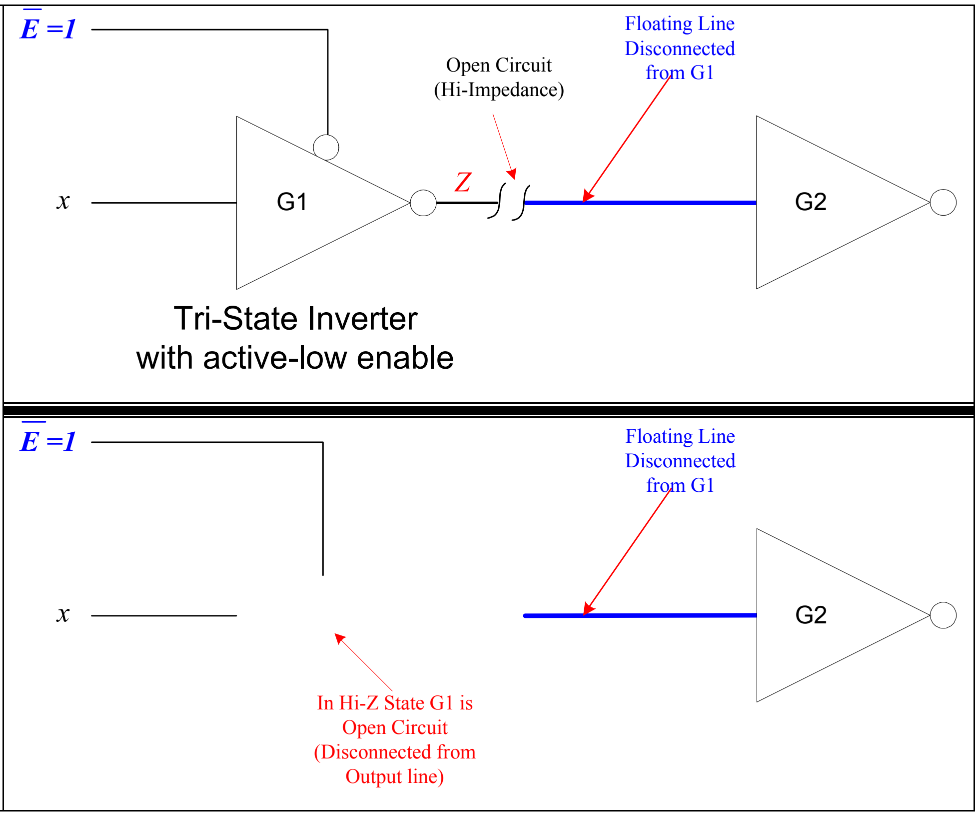
Truth Table

$\overline{E}$	x	Z
0	0	1
0	1	0
1	0	Hi-Z
1	1	Hi-Z

Enabled State



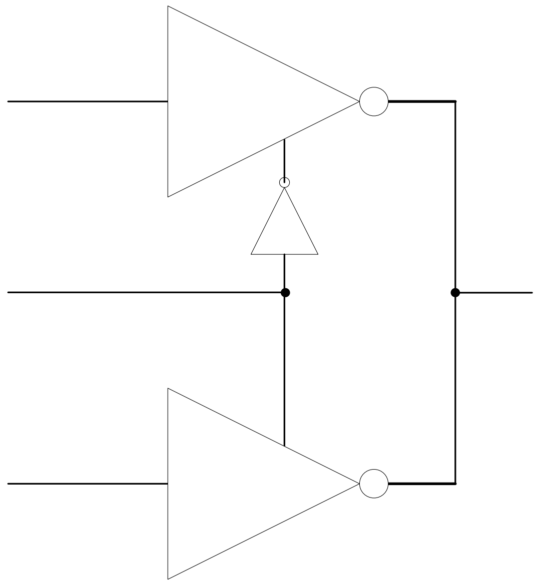
Dis-abled State



Condition for Connecting Outputs of Tri-State Gates

- Two or more tri-state *outputs* may be connected provided that *at most one* of these outputs is *enabled* while *all others are in the Hi-Z state*.
- This avoids conflict situations where one gate output is high while another is low.

Circuit Examples



- The shown circuit has tri-state inverters with active high enable inputs.
- The outputs of these 2 inverters are shorted together as a common output signal Z
- The 2 gates are NEVER enabled at the same time.
- G1 is enabled when E=1, while G2 is enabled when E=0
- The circuit performs the function: $Z = E\,\bar{x} + \bar{E}\,\bar{y}$