Name: **SOLUTION**
Student #: ________________

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COE 308 – Computer Architecture (T041)

Quiz # 03 – Solution

***** Show all your work. No credit will be given if work is not shown! *****

Problem # 1 (30 points): Assume a pipelined processor with 5 stages: Instruction Fetch (IF), Instruction Decode (ID), Operand Fetch (OF), Instruction Execute (IE), and Operand Store (OS). Consider the following code:

```
1.             LD    R1, 3         ; R1 ← 3
2.             LD    R2, 2         ; R2 ← 2
3.             LD    R3, –1        ; R3 ← –1
4.             ADD   R2, R2, R3    ; R2 ← R2 + R3
5.   Repeat:   SUB   R1, R1, R2    ; R1 ← R1 – R2
6.             BN    Skip          ; Branch to "Skip" if result is Negative
7.             SUB   R2, R1, R2    ; R2 ← R1 – R2
8.             SUB   R2, R2, R3    ; R2 ← R2 – R3
9.             BP    Repeat        ; Branch to "Repeat" if result is Positive
10.  Skip:     ADD   R3, R2, R3    ; R3 ← R2 + R3
```

(i) **(10 points)** Calculate the number of cycles to execute the code using a non-pipelined processor assuming that each instruction requires 5 cycles to execute. Show the contents of R1, R2, and R3 during the execution.

Instruction	R1	R2	R3
1	3		
2	3	2	
3	3	2	-1
4	3	1	-1
5	2	1	-1
6	Branch ***not*** taken		
7	2	1	-1
8	2	2	-1
9	Branch taken		
5	0	2	-1
6	Branch ***not*** taken		
7	0	-2	-1
8	0	-1	-1
9	Branch ***not*** taken		
10	0	-1	-2

\# cycles to execute = 15 × 5 = 75 cycles

(ii) **(15 points)** Use the following table to calculate the number of cycles to execute the code using the pipelined processor described above taking into account **data dependency**. Assume no forwarding hardware. Assume also that when a branch instruction is **fetched**, the pipeline is stalled until target address is calculated and branch decision is made. Assume delayed branch instruction scheme **not** being used.

Time unit	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20
OS					1	2	3			4			5	6				7		
IE				1	2	3			4			5	6				7			8
OF			1	2	3	***4***	***4,5***	4	***5,6***	***5,6***	5	6				7	***8***	***8,9***	8	9
ID		1	2	3	4	5	6								7	8	9			
IF	1	2	3	4	5	6								7	8	9				

Time unit	21	22	23	24	25	26	27	28	29	30	31	32	33	34	35	36	37	38	39
OS	8	9				5	6				7			8	9				10
IE	9				5	6				7			8	9				10	
OF				5	6				7	***8***	***8,9***	8	9				10		
ID			5	6				7	8	9						10			
IF		5	6				7	8	9						10				

(iii) **(5 points)** Calculate the speedup.

Speedup = (# cycles to execute using non-pipelined processor) / (# cycles to execute using pipelined processor)
= 75 / 39 = 1.923