

Name: **SOLUTION**
Student #: _____

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COE 308 – Computer Architecture (T032)

Quiz # 02 (SOLUTION)

***** Show all your work. No credit will be given if work is not shown! *****

Problem # 1: Consider a computer system that has a cache consisting of 64 blocks. The MM contains 512K blocks, each consisting of 32 bytes. Answer the following assuming (i) fully associative cache, (ii) direct cache, then (iii) set associative with four-block sets:

1. How many bits are needed for the MM address?
2. How many bits are needed for each of the TAG, SET, and WORD fields?

Solution:

$$\text{MM size} = 512\text{K} \times 32 = 2^{24}$$

(i) Fully Associative:

1. # MM address bits = $\lceil \log_2 \text{MM size} \rceil = \lceil \log_2 2^{24} \rceil = 24$ bits
2. # WORDs per block = 32 bytes
SETs = 1
TAGs = # MM blocks / # SETs = $512\text{K} / 1 = 512\text{K} = 2^{19}$

$$\begin{aligned} \Rightarrow \# \text{ WORD field bits} &= \lceil \log_2 32 \rceil &&= 5 \text{ bits} \\ \Rightarrow \# \text{ SET field bits} &= \lceil \log_2 1 \rceil &&= 0 \text{ bits} \\ \Rightarrow \# \text{ TAG field bits} &= \lceil \log_2 2^{19} \rceil &&= 19 \text{ bits} \end{aligned}$$

(ii) Direct:

1. # MM address bits = $\lceil \log_2 \text{MM size} \rceil = \lceil \log_2 2^{24} \rceil = 24$ bits
2. # WORDs per block = 32 bytes
SETs = 64
TAGs = # MM blocks / # SETs = $512\text{K} / 64 = 8\text{K} = 2^{13}$

$$\begin{aligned} \Rightarrow \# \text{ WORD field bits} &= \lceil \log_2 32 \rceil &&= 5 \text{ bits} \\ \Rightarrow \# \text{ SET field bits} &= \lceil \log_2 64 \rceil &&= 6 \text{ bits} \\ \Rightarrow \# \text{ TAG field bits} &= \lceil \log_2 2^{13} \rceil &&= 13 \text{ bits} \end{aligned}$$

(i) Set Associative: Four-block sets \Rightarrow 4-way set associative

1. # MM address bits = $\lceil \log_2 \text{MM size} \rceil = \lceil \log_2 2^{24} \rceil = 24$ bits
2. # WORDs per block = 32 bytes
SETs = $64 / 4 = 16$
TAGs = # MM blocks / # SETs = $512\text{K} / 16 = 32\text{K} = 2^{15}$

$$\begin{aligned} \Rightarrow \# \text{ WORD field bits} &= \lceil \log_2 32 \rceil &&= 5 \text{ bits} \\ \Rightarrow \# \text{ SET field bits} &= \lceil \log_2 16 \rceil &&= 4 \text{ bits} \\ \Rightarrow \# \text{ TAG field bits} &= \lceil \log_2 2^{15} \rceil &&= 15 \text{ bits} \end{aligned}$$

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Problem # 2: Using the ageing counters to implement the LRU algorithm, derive the numbers held in the counters after each in the following sequence (use the table below):

7, 5, 1, 5, 1, 1, 1, 5, 7, 2, 5, 5, 6, 1, 7, 6

Furthermore, calculate the hit ratio for the sequence given above. Assume that the cache consists of four blocks. Assume also that initially the cache is empty, and when filling the cache **initially** the block filling sequence is block 0, block 1, block 2, and finally block 3.

Address Tag	Hit/Miss	C ₀	C ₁	C ₂	C ₃	Subsequent actions
Initialization		0	0	0	0	
7	Miss	0	1	1	1	Block 0 filled
5	Miss	1	0	2	2	Block 1 filled
1	Miss	2	1	0	3	Block 2 filled
5	Hit	2	0	1	3	Block 1 accessed
1	Hit	2	1	0	3	Block 2 accessed
1	Hit	2	1	0	3	Block 2 accessed
1	Hit	2	1	0	3	Block 2 accessed
5	Hit	2	0	1	3	Block 1 accessed
7	Hit	0	1	2	3	Block 0 accessed
2	Miss	1	2	3	0	Block 3 filled
5	Hit	2	0	3	1	Block 1 accessed
5	Hit	2	0	3	1	Block 1 accessed
6	Miss	3	1	0	2	Block 2 replaced
1	Miss	0	2	1	3	Block 0 replaced
7	Miss	1	3	2	0	Block 3 replaced
6	Hit	2	3	0	1	Block 2 accessed

Hit ratio = 9 / 16 = 0.5625