King Fahd University of Petroleum and Minerals
College of Computer Sciences and Engineering
Department of Computer Engineering

COE 308 – Computer Architecture (T032)

Homework # 02 (SOLUTION)

A 64-bit processor with a 16-bit wide data bus is connected to 4 memory modules. Each module is 32 KBytes. Answer the following questions assuming ***(i)*** low order memory interleaving (all memory modules use the same set of addresses, and contents of each memory module are not necessarily the same as the contents of the other memory modules), ***(ii)*** low order memory interleaving (each memory module uses a unique set of addresses), then ***(iii)*** high order memory interleaving:

1- What is the minimum size of the address bus?
2- For maximum operand size, **and starting at memory location 0**, how many bytes the processor should fetch from each module to complete a computation?
3- Show the memory map for storing the integer (**0×7C58A4234588BF19**) at memory location **0** using **big-endian** addressing.

Solution:

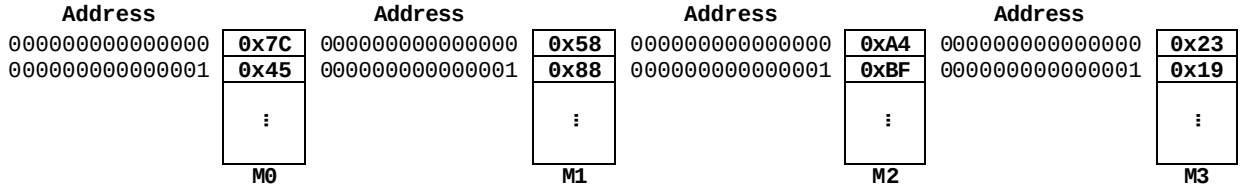
1-

(i) low order memory interleaving (same set of addresses)	(ii) low order memory interleaving (different set of addresses)	(iii) high order memory interleaving
$\log_2 (32 * 1024) = 15$ bits	$\log_2 (4 * 32 * 1024) = 17$ bits	$\log_2 (4 * 32 * 1024) = 17$ bits

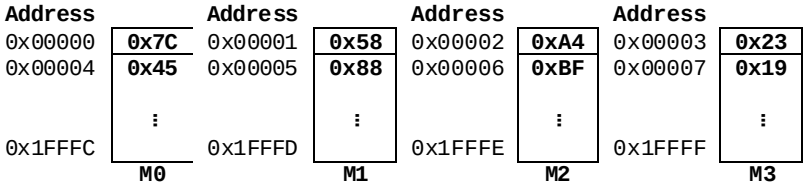
2- Since the processor is a 64-bit processor, then the maximum operand size is 64-bits = 8 bytes.

(i) low order memory interleaving (same set of addresses)	(ii) low order memory interleaving (different set of addresses)	(iii) high order memory interleaving
each module supplies 2 bytes	each module supplies 2 bytes	1st module supplies 8 bytes and the other modules supply 0 bytes

3- **i. low order memory interleaving (same set of addresses, not the same contents)**



ii. low order memory interleaving (different set of addresses)



iii. high order memory interleaving