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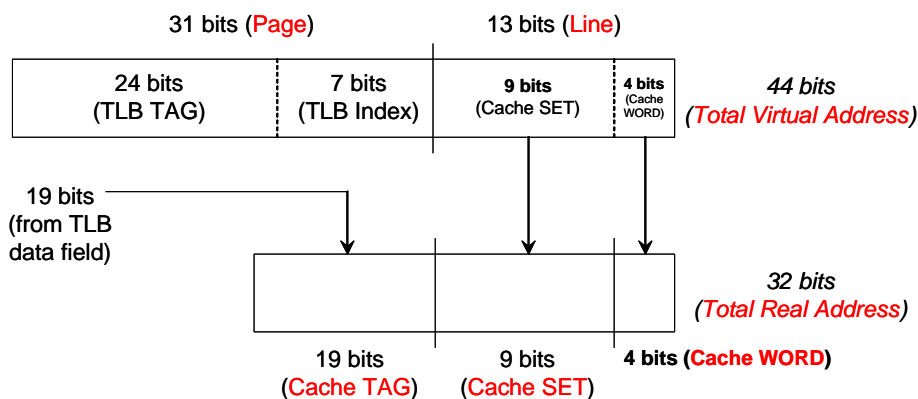
COE 308 – Section 02 – Computer Architecture (T032)

A system has both a virtual memory and a real address data cache, with the following characteristics:

- 44-bit virtual address
- 32-bit real address
- 8 Kbyte pages
- 2-way set associative TLB with 256 entries in total
- 4-way set associative data cache with 2048 blocks in total
- Each block consists of 16 words

- (i) Show the division of bits in the real address (i.e. Cache TAG, SET, and WORD sizes), and in the virtual address (i.e. Page TAG, Page INDEX, SET, and WORD sizes).

To find the “Line” field: Each page size is 8 KBytes = 2^{13} \Rightarrow “Line” bits = 13 bits
 To find the “Page” field: There are $(2^{44} / 8 \text{ Kbytes}) = 2^{31}$ virtual pages (where 44 is the size of the virtual address) \Rightarrow “Page” bits = 31 bits
 To find the TLB “Index” field: The TLB has 256 entries with 2-way set associative mapping, i.e. $256 / 2 = 128$ sets \Rightarrow TLB “Index” bits = 7 bits
 To find the TLB “Tag” field: There are 2^{31} virtual pages mapped to 128 (i.e. 2^7) TLB sets \Rightarrow TLB “Tag” bits = $\log_2(2^{31} / 2^7) = 24$ bits
 To find the “WORD” field: Each block of cache consists of 16 words \Rightarrow “WORD” bits = 4 bits
 To find the “SET” field: The cache has 2048 blocks with 4-way set associative mapping, i.e. $2048 / 4 = 512$ sets \Rightarrow “SET” bits = 9 bits
 To find the cache “TAG” field: There are $2^{32} / 16 = 2^{28}$ MM blocks mapped to 512 (i.e. 2^9) cache sets \Rightarrow cache “TAG” bits = $\log_2(2^{28} / 2^9) = 19$ bits (note: 0 bits are from “Line” field, and 19 bits from data field of TLB entry)



- (ii) How many virtual pages are there in the system? How many real pages are there in the system?

virtual pages = $2^{44} / 8 \text{ Kbytes} = 2^{31}$ pages, and # real pages = $2^{32} / 8 \text{ Kbytes} = 2^{19}$ pages