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COE 308 – Section 02 – Computer Architecture (T032)

A system has both a virtual memory and a real address data cache, with the following characteristics:

44-bit virtual address

32-bit real address

8 Kbyte pages

2-way set associative TLB with 256 entries in total

4-way set associative data cache with 2048 blocks in total

Each block consists of 16 words

- (i) Show the division of bits in the real address (i.e. Cache TAG, SET, and WORD sizes), and in the virtual address (i.e. Page TAG, Page INDEX, SET, and WORD sizes).

- (ii) How many virtual pages are there in the system? How many real pages are there in the system?