Principles of VLSI Design COE 360 (3-0-3)
Course Outline

Course Description

MOS Transistor operation and limitations, MOS digital logic circuits (NMOS & CMOS), static & dynamic logic, combinational and sequential circuits, propagation delay, transistor sizing, MOS IC fabrication, layout and design rules, stick diagrams, IC Design and Verification Tools, subsystem design and case studies, and practical considerations.

Prerequisite: EE 203.

Text Book: S.-M. Kang and Y. Leblebici, *CMOS Digital Integrated Circuits: Analysis and Design*, 2nd ed., 1999. Also some handouts on basic semiconductor concepts will be used insha'Alla.

References: 1) N. Weste and K. Eshraghian, *Principles of CMOS VLSI Design*, Addison Wesley, 1993.
2) Ken Martin, *Digital Integrated Circuit Design*, Oxford Press, 2000.
3) Jan Rabaey, *Digital Integrated Circuits; A design Perspective*, Prentice Hall, 1996.

Course Rationale

This course teaches the fundamental issues involved in the design, verification and manufacturing of digital integrated circuits (ICs).

Grading Policy

Grading is meant only as a way of assessing the student's achievements in the course. Students should not feel too much pressured by this process. The adopted grading policy allows and indeed rewards improvements. A student failing to achieve a good grade in the first exam should not feel that he has no chance. The whole purpose of the adopted grading policy is to give the student a second and even a third chance if he needs it to achieve the best result he wants.

Assignments & Quizzes	10 points
Project	20 points
Exam I	15 points
Exam II	15 points
Final Exam	40 points
Total	100 points

Attendance Policy

- Attendance will be taken regularly. Students who are more than 10 minutes late are considered absent,
- There will be a 0.5% grade deduction for every unexcused absence,
- Excuses for officially authorized absences must be presented no later than one week following resumption of class attendance.

Relevant Program Outcomes:

The following program outcomes have been identified as being served by this course (to various degrees):

1. (a) an ability to apply knowledge of mathematics, science, and engineering **(low service)** → energy bands formation, deriving drain current equation, circuit delay equations, optimization of buffer chains → a total of less **than 5%** of the course contents/outcomes

2. (b) an ability to design and conduct experiments, as well as to analyze and interpret data **(Low Service?)** → could SPICE simulations be counted as experimentation? Or it fits more under (e) (k)???

3. (c) an ability to design a system, component, or process to meet desired needs **(High Service)** → Circuit Design for certain specifications (Delay, power, area, Noise margins ..etc.)

4. (d) an ability to function as an effective team member **(Medium Service)** → The project, medium level since the project does not contain many tasks/team members

5. (e) an ability to identify, formulate, and solve engineering problems **(Low to zero Service?)** → usually project specs are well defined and supplied by the instructor!

6. (g) an ability to communicate effectively **(Low Service)** → The project report (written communication)

7. (k) an ability to use the techniques, skills, and modern engineering tools necessary for engineering practice **(Medium Service)** → The project, medium level since the project does not contain many tasks/engineering tools such as project planning/monitoring tools, design database management tools …etc.

8. (n) The ability to design and analyze IT (Information Technology) solutions for the Saudi Arabian market including the design and/or the integration of different hardware and software components **(low Service)** → understanding the environmental factors (such as Temperature) impact on IC performance and scaling of CMOS circuits (with compatibility issues and different voltage and I/O standards)???

Course Learning Outcomes

1. Knowledge of Semiconductor material properties and how they relate to their atomic structure and how they can be utilized to make useful devices (Diodes and MOS switches) → (a) → Evaluation through assignments and exams

2. A deep understanding of the operation of MOS transistors under different conditions (voltage, temperature and scaling) using adequate models while realizing the limitations of these models → (a), (e) and (k) → Evaluation through assignments and exams

3. Ability to use MOS transistors to construct useful circuits that achieve the required functionality → (a), (b), (c), and (e)→ Evaluation through assignments, exams and project

4. Ability to Design, Verify, Analyze and Evaluate the performance (speed, Power, Area, Noise margins) of different MOS digital circuits under different operating conditions → (a), (b), (c), (e), (k) and (n) → Evaluation through assignments, exams and project

5. Knowledge of the basic CMOS manufacturing process → (c) → Evaluation through assignments and exams

6. Ability to produce an efficient mask design (layout, or blue print) of a CMOS IC for certain specifications (functional, speed, constraints ...etc.). This would involves such skills as design segmentation, simple floor planning, layout and post layout verification → (b), (c), (e) and (k) → Evaluation through assignments, exams and project

7. Ability to use CAD tools relevant to IC design → (k)

8. Ability to professionally document design activities and results → (g) → Project report

9. Ability to work in a team → (d) → Project

Learning Methodology

The course objective shall be met insha'Allah though lectures, hands-on in-class exercises, assignments, project and the use of software for simulations and design of MOS chips.

Course Topics:

1. ***Review Material:*** **(2 weeks)**
   - Types of solids (in terms of conductivity)
   - Review of basic semiconductor concepts (types, doping, Electrons and holes, calculating n and p, Mobility, conductivity, current transport)
   - PN junction (structure, built-in potential, I-V characteristics, and capacitance).

2. ***The MOS Transistor:*** **(3 weeks)**
   - Structure (NMOS, PMOS, Enhancement vs. depletion)
   - Operation (regions and basic equations)
   - Limitations and scaling effects (Body effect, Latchup, Velocity saturation, Drain-Induced Barrier lowering (DIBL), Hot Electrons injection, and leakage)
   - SPICE models and capacitances

3. ***Digital MOS Circuits:*** **(5 weeks)**
   - Review of basic Specifications of Digital Integrated Circuits (Noise Margins, Fanin, Fanout and Power dissipation).
   - Static MOS inverters (NMOS and CMOS inverters, delay models, transistor sizing, and power dissipation)
   - Static NMOS & CMOS logic, pass-transistor logic (PTL), transmission gates, differential Cascode Static Logic (DCSL), Latches and registers
   - Dynamic MOS Logic (Domino Logic, Dynamic DCL, Charge Sharing and True Single-Phase Clock (TSPC)

4. ***CMOS Processing Technology:*** **(3 weeks)**
   - Photolithography and masking
   - CMOS fabrication process (epitaxy, oxidation, diffusion, implantation, metalization and passivation)

- CMOS design rules and layout (transistors, interconnects, Sheet resistance, integrated resistors and capacitors, and Distributed RC Effect)

5. ***CMOS IC Design & Case Studies***: **(2 weeks)**
   - Subsystem Design (Floor planning, Adders, shifters, ALUs, decoders, counters, Memories, I/Os and case studies)
   - ***VLSI Design Styles*** (Custom vs. Semicustom techniques, Standard Cells, Gate Arrays, FPGAs and testing)

Course Project: The course project is a very important tool to develop and apply different concepts learned in the course. It should also enhance the student's presentation skills and ability to work within a group. Groups of 1 to 3 students shall be formed and each will be assigned a different project. Each group shall divide the work among them and present their progress throughout the project phases.