coupled to a source follower stage comprising a plurality of pairs of PMOS transistors, the PMOS transistors providing a load means;

an input signal means and the reference voltage V_{ref} generating means being coupled respectively to the bases of the first and second of BJTs;

the load control means being coupled to the gates of the PMOS transistors, first and second control voltages V1 and V2 for biasing corresponding pairs of gates of the PMOS transistor pairs of the load means.

12. A circuit according to claim **11** wherein N wells of the PMOS transistors of the load means are coupled to the higher of the termination voltage V_T and supply voltage V_{DD} through another pair of PMOS transistors.

13. A circuit according to claim **11** wherein the means for generating a reference voltage comprises

a voltage multiplier circuit comprising a bipolar junction transistor Q1;

a first MOS transistor which is ON only for V_T less than a predetermined value, the first MOS transistor being coupled to the voltage multiplier circuit;

and temperature compensation means comprising a second MOS transistor coupled to a diode, the temperature compensating means being coupled to the voltage multiplier circuit and the first MOS transistor;

the second MOS transistor being biased in such away that its drain current increases linearly with V_T thereby keeping the current through the BJT Q1 in the voltage multiplier circuit constant, whereby V_{ref} is independent of V_T.

14. A circuit according to claim **11** for chip-to-chip communication over a transmission line with termination voltage V_T wherein the reference voltage V_{ref} is held by the V_{ref} generating means at about −0.45V below the termination voltage V_T.

15. A circuit according to claim **11** wherein the load control means is operable to provide first and second control voltages for biasing the PMOS load devices whereby the BJT pair do not saturate.

16. A circuit according to claim **11** wherein the load control means comprises a source coupled NMOS transistor pair coupled to cross coupled PMOS transistor loads.

17. An BiMOS integrated circuit comprising a driver circuit for a transceiver for high speed chip-to-chip communications, the driver circuit comprising:

current source means comprising a dynamically controlled biasing network for generating a control voltage V_c from an input signal whereby the low value of an output current is near zero and the high value of an output current is independent of the voltage swing of the input signal, the dynamically controlled biasing network comprising a V_{BE} multiplier having a first bipolar transistor Q1 biased by first resistor R and second resistor zR where z is the multiplication factor, wherein z is selected to provide a near zero tail current.

18. A driver circuit according to claim **17** wherein the current source means comprises a bipolar transistor Q3 and an emitter coupled Resistance R_s, the dynamically controlled biasing network providing a control voltage V_c for biasing the base of a bipolar transistor Q3 of the current source means.

19. A driver circuit according to claim **17** comprising another BJT (Q4), which is much smaller than Q3, emitters of Q3 and Q4 being coupled together, the collector of Q4 being coupled to the supply voltage, the base of Q4 being coupled to another reference voltage source.

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