and for UOD2, circuit **600**, in the upper trace. The on-chip power requirements at that frequency were 75 mW and 80 mW for the UOD1 and the UOD2, respectively. The measured output of UOD1 at 1 GHz and 5V termination is shown in FIG. **13**. The power of a CML driver at the same termination voltage is about 125 mW. For comparison an ECL or pseudo ECL driver would dissipate an even greater power under the same conditions.

For a 2V termination power dissipation of the UOD1 and UOD2 are 25 mW and 29 mW respectively. Simulations showed the superior speed performance of UOD2 over the V_T range. Also, for both drivers, the maximum frequency of operation decreased as VT decreased due to the increase of the collector capacitance and the saturation effects of Q3 (FIG. **14**).

Thus a BiCMOS transceiver has been developed which can operate without the need for an off-chip reference voltage. All the required referencing and biasing voltages are generated on chip. Operating with a 3.3 V supply, signals can be received with termination voltages from 1.5 to 5V at frequencies up to and exceeding 1.5 GHz. The driver can operate at frequency above 1 GHz with termination voltage ranging from 2V to 5V. Thus the driver and receiver are operable over a range of termination voltages which is wide enough to be considered universally compatible with various types of integrated circuits. The on-chip power of both receiver and driver are well below that of known CML/ECL transceivers of comparable speeds. Thus the capabilities of BiCMOS technology in implementing diversified high performance smart I/Os and voltage referencing circuits are demonstrated.

Although particular embodiments of the invention have been described in detail, it should be appreciated that numerous modifications, variations and adaptations may be made without departing from the scope of the invention as defined in the claims.

What is claimed is:

1. A transceiver for high speed chip to chip communications over a transmission line with termination voltage V_T, comprising a driver circuit and a receiver circuit, wherein the receiver circuit comprises:

an input buffer (UIB);

means for generating a reference voltage (V_{ref});

and load control means for generating first and second control voltages V1 and V2;

the input buffer comprising an emitter coupled differential pair of first and second bipolar junction transistors (BJTs) coupled to a source follower stage comprising a plurality of pairs of PMOS transistors, the PMOS transistors providing a load means;

an input signal means and the reference voltage V_{ref} generating means being coupled respectively to the bases of the first and second of BJTs;

the load control means being coupled to the gates of the PMOS transistors, for providing first and second control voltages V1 and V2 for biasing corresponding pairs of gates of the PMOS transistor pairs of the load means.

2. A transceiver according to claim **1** wherein N wells of the PMOS load means are coupled to the higher of the termination voltage V_T and supply voltage VDD through another pair of PMOS transistors.

3. A transceiver according to claim **1** wherein the means for generating a reference voltage comprises

a voltage multiplier circuit comprising a bipolar junction transistor Q1;

a first MOS transistor which is ON only for V_T less than a predetermined value, the first MOS transistor being coupled to the voltage multiplier circuit;

and temperature compensation means comprising a second MOS transistor coupled to a diode, the temperature compensating means being coupled to the voltage multiplier circuit and the first MOS transistor;

means for biasing the second MOS transistor to provide a drain current that increases linearly with V_T thereby maintaining a current through the BJT Q1 in the voltage multiplier circuit constant, whereby V_{ref} will always is independent of V_T.

4. A transceiver according to claim **1** for chip-to-chip communication over a transmission line with termination voltage V_T wherein the reference voltage V_{ref} is held by the V_{ref} generating means at about −0.45V below the termination voltage V_T.

5. A transceiver according to claim **1** wherein the load control means biases the PMOS load devices such that the input BJT pair never saturates.

6. A transceiver according to claim **1** wherein the load control means comprises a source coupled NMOS transistor pair coupled to cross coupled PMOS transistor loads.

7. A transceiver comprising a receiver circuit and a driver circuit, wherein the driver comprises:

current source means comprising a dynamically controlled biasing network for generating a control voltage V_c from an input signal whereby the low value of an output current is near zero and the high value of an output current is independent of the voltage swing of the input signal, the dynamically controlled biasing network comprising a V_{BE} multiplier having a first bipolar transistor Q1 biased by first resistor R and second resistor zR where z is the multiplication factor, wherein z is selected to provide a near zero tail current.

8. A transceiver according to claim **7** wherein the current source means comprises a bipolar transistor Q3 and an emitter coupled Resistance R_s, the dynamically controlled biasing network providing a control voltage V_c for biasing the base of a bipolar transistor Q3 of the current source means.

9. A transceiver according to claim **8** comprising another BJT (Q4), which is much smaller than Q3, emitters of Q3 and Q4 being coupled together, the collector of Q4 being coupled to the supply voltage, the base of Q4 being coupled to another reference voltage.

10. A transceiver comprising a receiver circuit and a driver circuit,

the receiver circuit comprising an input buffer comprising an emitter coupled bipolar junction transistor pair, and source follower stage comprising a plurality of PMOS load devices, voltage generating means for providing a reference voltage and load control means for generating first and second control voltages for biasing the PMOS load devices whereby the first and second BJTs do not saturate; and

the driver circuit comprising a current source means having a dynamically controlled biasing network.

11. A BiCMOS integrated circuit comprising a receiver circuit for a transceiver for high speed chip-to-chip communications over a transmission line with termination voltage V_T, the receiver circuit comprising:

the receiver circuit comprises:

an input buffer (UIB);

means for generating a reference voltage (V_{ref});

and load control means for generating first and second control voltages V1 and V2;

the UIB comprising an emitter coupled differential pair of first and second bipolar junction transistors (BJTs)