Experimental results showing the measured output waveforms of an ECL driver being driven by the receiver at 1.5 GHz (FIG. **15**) showing the ability to switch the ECL driver and operate at this frequency. The input signal was terminated to 2V and the value of the tail current of the UIB used was 1 mA.

The measurements showed that the receiver successfully read signals with termination voltages ranging from 1.5 to 5V and frequencies exceeding 1.5 GHz.

Output Driver

An output driver **500** according to a first embodiment of the present invention, UOD**1**, is shown in FIG. **10** and an output driver **500** according to a second embodiment of the present invention, UOD**2**, is shown in FIG. **11**.

As mentioned above, conventionally, a CML driver is used when lower power is required. The tail current value is determined by the value of the termination resistance and the required output voltage swing. Hence for a 50 Ω termination and a 0.8V swing, the value of the tail current has to be set around 16 mA. This not only limits the speed of the driver but also wastes power. When the output is high and the tail current is in the other branch of the current switch, assuming a single ended output, a high current is not required for operation of the circuit.

An improved current source, which includes a dynamically controlled biasing network and overcomes these shortcomings is shown in FIG. **17**, with the conventionally used current source shown for comparison in FIG. **16**. The current source developed for the output drivers according to the first and second embodiments were developed from the improved current source of FIG. **17**, and thus the latter circuit will be described in detail first.

The improved current source works as follows: voltage V_c which in conjunction with resistor R_s determines the value of the tail current is equal to the difference between the voltages at V_a and V_b. When the input I/P is high V_c is given by:

$$V_{chigh}=z\cdot V_{BE}.$$

where z is the multiplication factor of the V_{BE} multiplier which comprises Q**1** and the two resistors R and zR (FIG. **17**). z is adjusted such that V_c is about 1.2 to 1.3V (i.e. z is from about 1.5 to 1.8) and Rz is adjusted such that the high value of the current is around 16 mA. When I/P is low, V_c becomes:

$$V_{clow}=(z-x+1)\cdot V_{BE}$$

where x is the multiplication factor of the V_{BE} multiplier which comprises Q**2** and the two resistors R**2** and xR**2** (FIG. **17**) and is between 1.2 to 1.3. Also, it is assumed that the input voltage swing V_s is larger than $\{(x-1)\cdot V_{BE}\}$ such that the low value of the tail current which is determined by the value of V_c in equation above is independently of the voltage swing.

The low value of the tail current constitutes a trade-off between power and speed. The smaller this value, the lower the power is, and the longer the time it takes to boost the current to the high value and switch the circuit. The capacitances C_x are used to enhance the speed and resolve to some degree, the trade-off just described. They do not affect the DC characteristics. The biasing network boosts the tail current during the pull down transition. The driver with the dynamic active pull down current source circuit consumes 40% less power than that of a CML driver with the conventional current sourcing circuit. Also for typical operating conditions, e.g. burst modes, the DCCP circuit saves idle power as compared to the conventional current source circuit. DCCP may be used similarly to reduce the power of an ECL driver by reducing the power consumption in the current switch. Application of this technique to a current source for the output drivers according to embodiments of the present invention will now be described.

An output driver **500** according to a first embodiment of the present invention, UOD**1**, is shown in FIG. **10**. Comparing this circuit schematic with that of the dynamically controlled charge pumped (DCCP) current source circuit described above with reference to FIG. **17**, it will be seen that UOD**1** is similar in many respects, and results from a modification of the circuit so that the low value of the tail current becomes zero. This is achieved by removing Q**2**, R**2** and xR**2** from the circuit in FIG. **17**, so that the following condition is imposed by the design:

$$1<z\leqq 1+V_S/V_{BE}$$

where Vs is the voltage swing of the input signal. This requirement sets the output current LOW value to zero. When I/P is LOW, Vc would be $\leqq V_{BE}$. When I/P is HIGH

$$V_c high=zV_{BE}+Vs.$$

(V_c would be $\leqq V_{be}$ when I/P is low). Thus an approximate value of V_s should be known in advance for proper design of the driver. Note that the HIGH value of the output current, and consequently the output swing, is independent of the exact value of V_s.

In practice, the circuit **500** of UOD **1** has two shortcomings. Firstly, the large BJT Q**3** is turned on/off solely through the base, hence the base resistance R_b makes the turn on/off slower than the combined base/emitter turn-on/off, as in CML/ECL circuits described above. Secondly, the LOW value of the output current might not be exactly zero as intended in the design. It may reach a few hundreds of μA due to tolerances of resistors in the biasing network, which would slightly reduce noise margins by reducing the value of the output high value V_OH.

A universal output driver **600** according to a second embodiment of the present invention UOD**2** is shown in FIG. **11**. The circuit is similar to the circuit **500** of FIG. **10** UOD**1**, with the addition of another BJT, Q**4** as shown in FIG. **11**. Q**4**, is much smaller than Q**3**, and has its base connected to a reference voltage V_r. In this circuit, the restriction on the HIGH limit of z is relaxed since the LOW value of V_c (V_c low) does not have to be less than V_{BE}. The high value of V_c is still equal to zV_{BE}.

When the input I/P goes LOW, the tail current is steered away from Q**3** to Q**4**. The LOW value of the tail current however is much smaller than the HIGH value because 1) V_r is set to a value less than the HIGH value of V_c; and 2) V_{BE} of Q**4** is larger than that of Q**3**.

Hence, the voltage across R_s will be much smaller when I/P is low. When I/P becomes HIGH, the LOW tail current is steered away from Q**4** to Q**3**, and helps turning-on Q**3**.

Also, since V_c low can be made greater than that of the UOD**1**, without affecting the V_oH and the noise margins, the voltage swing of V_c may be made smaller, and hence the circuit operates faster.

The advantages of the driver of the second embodiment UOD**2** relative to the UOD **1** is obtained with a slight increases in power consumption and area.

The measured outputs of the drivers of the first and second embodiments at 0.5 GHz and a termination voltage of 5V are shown in FIG. **12** for UOD**1**, circuit **500**, in the lower trace,