DESCRIPTION OF THE PREFERRED EMBODIMENTS

A generalized schematic diagram of a transceiver **10** comprising a transmitter **12** and a receiver **14** interconnected by a transmission line **16** for transmitting and receiving digital signals for high speed chip-to-chip communications is shown schematically in FIG. **1**. The transmitter **12** forms part of an integrated circuit comprising signal transmitting circuitry **18** and an output driver **20**, and the receiver **14** forms part of an integrated circuit comprising an input buffer **22**, and signal receiving circuitry **24**. The transmitter **12** converts the logic level of an input signal from a signal source, i.e. provided by the signal transmitting circuitry **18**, and the transmitted signal is transmitted along the transmission line **16** by the output driver **20**. The transmitted signal is received by the input buffer **22** of the receiver **14** for buffering or level shifting to provide a signal compatible with the signal receiving circuitry **24**.

A BiCMOS transceiver **100** according to a first embodiment of the present invention comprises a transmitter and a receiver **114**, for sending and receiving digital signals on a transmission line **116** for high speed chip-to-chip communications (FIG. **2**). The receiver **114** comprises a universal input buffer **200**, voltage reference generator **300** and load control circuit **400**, and transmitter **112** comprises an universal output driver **500**, which will be described in detail in the following sections. The output driver and input buffer are referred to as universal in the sense that they are designed to be compatible with other circuits operating over the wide range of voltages. In particular, the transmitter **112** and receiver **114** are designed for operation from a 3.3V supply voltage. The receiver can read signals with termination voltages from 1.5 to 5V. The universal driver can drive an external 25 Ω line terminated to a voltage ranging from 2V to 5V is described in the following section. specified above. For both the driver and receiver circuits there is no need for an external reference voltage. The only restriction on the signals is that they swing from V_T to V_T-V_s (i.e. they are not level shifted). V_s was assumed to be between 0.8 and 1.0V. Receiver

As shown schematically in FIG. **2**, the receiver **114** according to a first embodiment of the invention comprises **3** sub-circuits: the universal input buffer UIB **200** (FIG. **3**), and two reference circuits, the Vref generator **300** (FIG. **4**); and the load control circuit **400** (FIG. **5**).

The UIB **200** (FIG. **3**) comprises an emitter coupled pair of bipolar junction transistors (BJT) **212** and **214**, followed by a source follower stage **216**. The four PMOS devices **M1**, **M2**, **M3** and **M4** (**218**,**220**,**222**,and **224**) serve as loads for the emitter coupled BJTs **212** and **214**. An input signal V_{in} and a reference voltage V_{ref} are applied respectively to the base of BJT **212** and the base of BJT **214**. The value of the reference voltage V_{ref} is held by the V_{ref} generator **300** (FIG. **4**) at about −0.45V below the termination voltage VT, assuming a signal voltage swing of 0.8 to 1.0V.

The PMOS load devices **218**,**220** **222** and **224** are controlled by the two biasing voltages **V1** and **V2**, which are generated by the load control circuit **400** (FIG. **5**).

The load control circuit **400** shows FIG. **5** generates the two control voltages **V1** and **V2** for biasing the PMOS load devices **218**,**220**,**222** and **224** such that the input BJT pair never saturates. For a termination voltage VT less than VDD (3.3V), **M1** (**218**) and **M4** (**222**) will be off, and **M2** (**220**) and **M3** (**224**) will be on and act as loads for the differential pair **212** and **214**. Similarly, when VT is greater than VDD, **M2** (**220**) and **M3** (**224**) will be off and **M1** (**218**) and **M4** (**222**) will be on.

Two additional PMOS transistors **M5** (**226**) and **M6** (**228**) ensure that the N wells of all the PMOS devices, **M1**–**M4** are connected to the highest voltage between VT and VDD. A source follower stage was used, instead of an emitter follower, to avoid saturation problems when VT is larger than VDD. While a source follower stage reduces the speed slightly, it ensures that the differential output signal will not saturate the driven gate.

The V_{ref} generator **300** (FIG. **4**) produces a stable reference voltage V_{ref} over a wide range of temperatures and for a range of VT from 1.5 to 5V. NMOSFET **Mn1** (**310**) in FIG. **2** is ON only for VT less than 2.5V. PMOSFET **Mp1** (**312**) and the diode **314** are used for temperature compensation. PMOSFET **Mp1** **312** is biased in such a way that its drain current will increase linearly with VT. This will keep the current through the BJT **Q1** (**316**) in the VBE multiplier circuit constant, and hence V_{ref} will always remain constant with respect to VT (i.e. V_{ref}=VT −0.45V).

As the temperature increases, the drain current of MOSFET **312** **Mp1** decreases and hence the emitter current of **Q1** **316** will increase and compensate the decrease in VBE that occurs as the temperature increases. The reverse happens when the temperature decreases.

FIG. **6** shows the stability of the measured output of the V_{ref} generator over a wide range of temperature for several termination voltages. The maximum change in V_{ref} over the whole temperature range shown for all values of termination voltages was 51 mV, or 5% of the voltage swing.

The load control circuit **400** (FIG. **5**) comprises a simple source coupled NMOS transistor pair **410** and **412** with cross-coupled PMOS loads **414** and **416**, for generating control voltages **V1** and **V2**.

This arrangement of the input and load MOS devices provides that when VT is less than VDD, **V1** will be HIGH and close to VDD (Vdd−**V1** would be less than the PMOS threshold voltage V_{tp}) and **V2** will be LOW. When Vt is greater than VDD, **V2** will be HIGH and close to VT (VT−**V2**<Vtp) and **V1** will be LOW. So for VT<VDD, **M1** and **M4** in the UIB are off, and **M2** and **M3** are on. Also **M5** will be on and the N wells will be connected to VDD.

If VT exceeds VDD, **M1** and **M4** will be turned on, **M1** and **M4** will be turned off, and the N wells will be connected to VT.

As VT increases further, **V2** keeps increasing such that **M2**, **M3** and **M5** remain off. This ensures the correct operation of the UIB. No current will flow between VT and VDD in any circumstances. The outputs of **V1** and **V2** versus VT are shown in FIG. **7** during correct operation.

The load control circuit was found to be very stable over the temperature range. The maximum change in **V1** and **V2** over the whole temperature range for any value of VT was found to be less than 10 mV.

The outputs of the UIB are shown in FIG. **8** for two values of VT (i.e. 2V and 5V) an input frequency of 1 GHz and an ECL gate as a fan out. The value of the tail current of the UIB was 1mA, and the total power of the receiver for a 3.3V termination voltage, including that of the biasing circuits at 1 GHz was 17 mW.

The maximum frequency of operation Fmax, (i.e. defined here as the frequency at which the output swing of the UIB becomes less than 250 mV) of the UIB versus the value of the tail current is shown in FIG. **9**.

In simulations, the sizes of the load PMOS devices **M1** to **M4** were proportionally increased with the tail current to keep the output voltage swing of the UIB constant. FIG. **9** shows that there is an optimum value of the tail current that yields a maximum speed.