first and second resistors, R and zR, where z is the multiplication factor, wherein z is selected to provide a near zero tail current.

Advantageously, another BJT (Q4) is added, which is much smaller than Q3, the emitters of Q3 and Q4 being coupled together, the collector of Q4 being coupled to the supply voltage, and the base of Q4 being coupled to another reference voltage. The additional elements assist in turning on and off the transistor Q3 more rapidly, thereby increasing the speed and improving noise margins.

These circuits are conveniently fabricated in submicron, e.g. 0.8 μm, BiCMOS technology, and may be operated using a supply voltage of 3.3V, i.e. a standard voltage for digital ASICs.

According to yet another aspect of the present invention there is provided a BiCMOS transceiver comprising a receiver circuit and a driver circuit,

the receiver circuit comprising:

an input buffer comprising an emitter coupled pair of first and second bipolar junction transistors (BJTs), and a source follower stage comprising a plurality of PMOS load devices, voltage generating means for providing a reference voltage and load control means for generating first and second control voltages for biasing the PMOS load devices whereby the BJT do not saturate; and

the driver circuit comprising a current source means having a dynamically controlled biasing network.

Using a supply voltage of 3.3V the transceiver can drive and receive low voltage swing signals with termination voltages ranging from 5V down to 2V without using an external reference voltages. Thus the transceiver is capable of accepting all commonly used signal levels of BiCMOS, ECL and CML circuits thus providing a "universal" transceiver for Gigahertz operation. Advantageously, on-chip power consumption is much lower than that of existing CML/ECL transceivers with comparable speed.

A further aspect of the present invention provides a BiCMOS integrated circuit comprising a receiver circuit for a transceiver for high speed chip-to-chip communications, the receiver circuit comprising: the receiver circuit comprises: an input buffer (UIB); means for generating a reference voltage (V_{ref}); and load control means for generating first and second control voltages V1 and V2; the UIB comprising an emitter coupled differential pair of first and second bipolar junction transistors (BJTs) coupled to a source follower stage comprising a plurality of pairs of PMOS transistors, the PMOS transistors providing a load means; an input signal means and the reference voltage V_{ref} generating means being coupled respectively to the bases of the first and second of BJTS; the load control means being coupled to the gates of the PMOS transistors, first and second control voltages V1 and V2 for biasing corresponding pairs of gates of the PMOS transistor pairs of the load means; and

Correspondingly, there is provided a BiCMOS integrated circuit comprising a driver circuit for a transceiver for high speed chip-to-chip communications, the driver circuit comprising: current source means comprising a dynamically controlled biasing network for generating a control voltage Vc from an input signal whereby the low value of the output current is near zero and the high value of the output current is independent of the voltage swing of the input signal.

Thus the driver and receiver may be used in conjunction with other driver and receivers of the same or different types because both the universal receiver and the universal driver are compatible with a wide range of high speed signals from many other common types of drivers and receivers. Thus an integrated circuit integrating a universal driver may be used transmitting signals for chip-to-chip communication with another integrated circuit comprising a different type of receiver circuit. Correspondingly, the universal receiver may receive signals over a wide range of voltages from other integrated circuits comprising drivers of other types. Thus incompatibilities due to different termination/reference voltage requirements and multiple termination and reference voltages, common in conventional systems using transceiver circuits, are avoided or reduced. By elimination or simplification of signal conversion, interface circuitry and multiple reference circuits, the complexity of the system is reduced with consequent overall cost savings.

BRIEF DESCRIPTION OF THE DRAWINGS

Embodiments of the invention will now be described by way of example, with reference to the accompanying drawings, in which:

FIG. **1** shows a schematic block diagram of a generalized prior art transceiver comprising a transmitter including a driver, and a receiver for chip-to-chip communications along a transmission line;

FIG. **2** shows a schematic block diagram of a transceiver comprising a transmitter including a driver, and a receiver for chip-to-chip communications along a transmission line according to a first embodiment of the present invention;

FIG. **3** shows a circuit schematic of a part of a receiver comprising a universal input buffer (UIB) according to a first embodiment of the present invention;

FIGS. **4** and **5** show circuit schematics of reference circuits comprising a reference voltage V_{ref} generator (FIG. **4**) and a load control circuit (FIG. **5**) according to a first embodiment of the invention;

FIG. **6** shows the measured output of the V_{ref} generator vs. temperature for several termination voltages;

FIG. **7** shows the outputs of the load control circuit vs. VT;

FIG. **8** shows the simulated UIB outputs for the two termination voltages at 1GHz and a fanout of one (ECL gate at the output);

FIG. **9** shows the maximum frequency of operation Fmax of the UIB vs. the tail current Iss.

FIG. **10** shows a circuit schematic comprising a universal output driver (UOD **1**) according to a first embodiment;

FIG. **11** shows a universal output driver (UOD **2**) according to a second embodiment.

FIG. **12** shows the measured output waveforms of the two drivers at 500 MHz and 5V termination: The output of UOD1 is the lower trace, and of UOD2 is the upper trace;

FIG. **13** shows the measured output waveforms of the output drivers of the first and second embodiments operating with an input signal of 500 MHz at a VT of 5V;

FIG. **14** shows the simulated maximum frequency of operation of the drivers of the first and second embodiments.

FIG. **15** shows the measured output waveforms of the receiver test structure at 1.5 GHz with 2V input signal termination and 20 dB attenuation at the input of the sampling scope;

FIG. **16** shows a prior art conventional CML driver comprising a conventional current source, and

FIG. **17** shows a CML driver having an improved current source according to an embodiment of the present invention.