BICMOS TRANSCEIVER (DRIVER AND RECEIVER) FOR GIGAHERTZ OPERATION

FIELD OF THE INVENTION

This invention relates to a BiCMOS transceiver (driver and receiver) for GHz operation.

BACKGROUND OF THE INVENTION

High speed digital telecommunications switches may comprise many interconnected integrated circuit (IC) chips. Chip-to-chip communication is achieved by transceivers, i.e. drivers and receivers, which transmit and receive signals along transmission lines interconnecting the integrated circuit chips. The demand for higher circuit speeds, higher chip-to-chip bit rates, and lower on-chip power consumption places corresponding demands the output drivers/input buffers of the transceivers. Low power consumption is essential to allow system designers to increase the number of I/Os per chip while maintaining high reliability and keeping the total power dissipation within thermal limits.

Bipolar circuits such as ECL (emitter coupled logic) or CML (current mode logic) can meet the speed requirements. ECL is conventionally used for maximum speed, while CML is used for lower power consumption. However, both CML and ECL, when used as drivers, consume large amounts of power, particularly for level shifting/buffering of the input signals, and for the current switch (the tail current). Thus low power consumption is an major concern as the number of I/Os for telecommunications integrated circuits increases.

Various dynamic circuits techniques to reduce power consumption of ECL/CML logic circuits, while maintaining or increasing their speeds, have been reported. However these techniques were intended for bipolar VLSI logic applications, and are not suitable for ECL/CML output driver applications.

Recently many low voltage swing driver circuits have been reported. These circuits range from reduced swing CMOS, CMOS pseudo ECL, or CMOS 100K ECL, and CMOS GTL. CMOS reduced swing transceivers have limited speed. CMOS pseudo ECL or CMOS 100K ECL are complicated and have higher power consumption. For example, CMOS GTL bi-directional transceiver is described in U.S. Pat. No. 5,023,488 to Gunning, entitled "Drivers and receivers for interfacing VLSI CMOS circuits to transmission lines" and requires different reference and termination voltages. Another transceiver having reduced EMI and power dissipation is described in copending U.S. patent application Ser. No. 08/368,945 filed Jan. 5, 1995 to Sasaki et al. entitled "Signal transmitter and transceiver and apparatus incorporating the same". However these receivers, as well as true or pseudo Bipolar ECL or CML transceivers, each require different termination voltages.

Thus, existing low voltage swing transceiver circuits are incompatible with each other due to their different termination/reference voltage requirements. In systems using parts with different transceiver types, signal conversion or interface circuitry, as well as multiple termination and reference voltages are required, which adds to the overall cost and complexity of the system.

Moreover, the Digital Signal Processing (DSP) portions of high speed communications chips are usually implemented using CMOS logic. As future submicron and deep submicron Bipolar CMOS technologies, are scaled down, the supply voltages will be scaled down, to maintain reliability of short channel MOS devices. Since BiCMOS technology combining bipolar and CMOS (complementary metal oxide semiconductor) technology has proven to be an excellent workhorse for telecommunications applications, there is a need for BiCMOS compatible transceivers capable of meeting the requirements mentioned above for high speed chip-to-chip communications.

SUMMARY OF THE INVENTION

Thus the present invention seeks to provide an improved transceiver, comprising driver and receiver circuits, with reduced power consumption and increased speed, which overcome or avoid the above-mentioned problems.

According to one aspect of the present invention there is provided transceiver for high speed chip to chip communications comprising a driver circuit and a receiver circuit, wherein the receiver circuit comprises: an input buffer (UIB); means for generating a reference voltage (V_{ref}); and load control means for generating first and second control voltages **V1** and **V2**; the input buffer comprising an emitter coupled differential pair of first and second bipolar junction transistors (BJTs) coupled to a source follower stage comprising a plurality of pairs of PMOS transistors, the PMOS transistors providing a load means; an input signal means and the reference voltage V_{ref} generating means being coupled respectively to the bases of the first and second of BJTs; the load control means being coupled to the gates of the PMOS transistors, for providing first and second control voltages **V1** and **V2** for biasing corresponding pairs of gates of the PMOS transistor pairs of the load means.

Preferably, N wells of the PMOS load means are coupled to the higher of VT and VDD through another pair of PMOS transistors, also controlled by first and second control voltages **V1** and **V2**.

The receiver can read signals with termination voltages from 1.5 to 5V and there is no need for an external reference voltage.

The means for generating a reference voltage comprises temperature compensation means whereby V_{ref} is independent of VT. Preferably, the reference voltage V_{ref} is held by the V_{ref} generating means at about –0.45V below the termination voltage VT of the transmission line. The load control means, which comprises a source coupled NMOS transistor pair and cross coupled PMOS transistor loads provides first and second control voltages **V1** and **V2** for biasing the PMOS load devices such that the input BJT pair never saturates.

According to another aspect of the present invention there is provided a transceiver for high speed chip-to-chip communications comprising a receiver circuit and a driver circuit, wherein the driver circuit comprises current source means comprising a dynamically controlled biasing network for generating a control voltage Vc from an input signal whereby the low value of the output current is set near zero and the high value of the output current is independent of the voltage swing of the input signal.

Thus, the driver can drive an external 25 Ω terminated to a voltage ranging from 2V to 5V, and an external reference voltage is not required.

Beneficially, the current source means comprises a bipolar transistor **Q3** and Resistance Rs and the dynamically controlled biasing network provides a control voltage Vc for biasing the base of a bipolar transistor **Q3** of the current source means.

The dynamically controlled biasing network comprises: a V_{BE} multiplier comprising a first bipolar transistor **Q1**, and