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United States Patent [19]

Elrabaa et al.

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[54] **LOW-POWER BICMOS/ECL SRAM**

[75] Inventors: **Muhammad S. Elrabaa**, Hillsboro, Oreg.; **Mohamed I. Elmasry**, Waterloo, Canada

[73] Assignee: **University of Waterloo**, Waterloo, Canada

[21] Appl. No.: **558,896**

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[51] **Int. Cl.**[6] **G11C 11/40**

[52] **U.S. Cl.** **365/177**; 365/189.05; 365/189.11; 365/189.08; 365/190; 365/205; 365/225.6; 365/230.06; 365/230.08

[58] **Field of Search** 365/177, 189.05, 365/189.11, 190, 205, 225.6, 227, 230.06, 230.08, 189.08

[56] **References Cited**

U.S. PATENT DOCUMENTS

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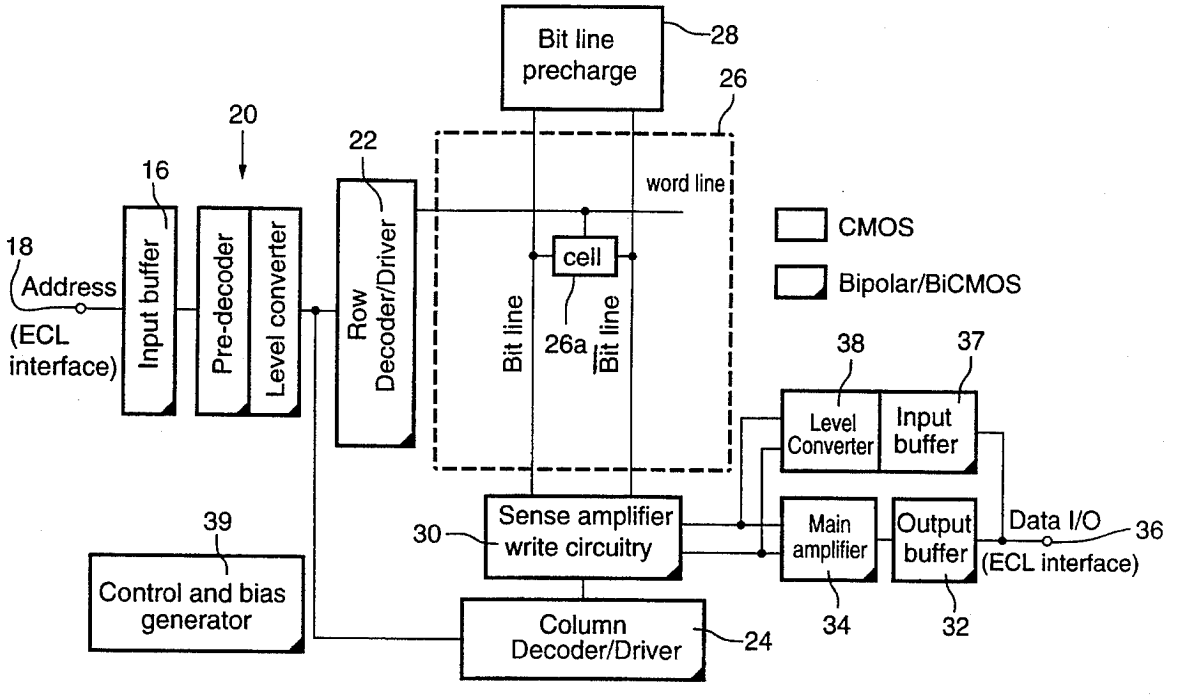
Primary Examiner—David C. Nelms
Assistant Examiner—Andrew Q. Tran
Attorney, Agent, or Firm—Connolly & Hutz

[57] **ABSTRACT**

A SRAM includes an ECL input buffer connected between an address bus and a W-OR predecoder array. The logic output of the W-OR predecoder array is applied to a level translator array and level shifted. The level shifted output of the level translator array is supplied to a plurality of self-resetting word-line decoder and driver (WLDD) circuits. The WLDD circuits supply activation pulses to selected blocks of memory in a memory cell array. Sense amplifiers sense and latch-in the data stored in the activated selected blocks of memory. The design of the W-OR predecoder array, level translator array, WLDD circuits and sense amplifiers is such to reduce the overall power consumption of the SRAM.

36 Claims, 9 Drawing Sheets



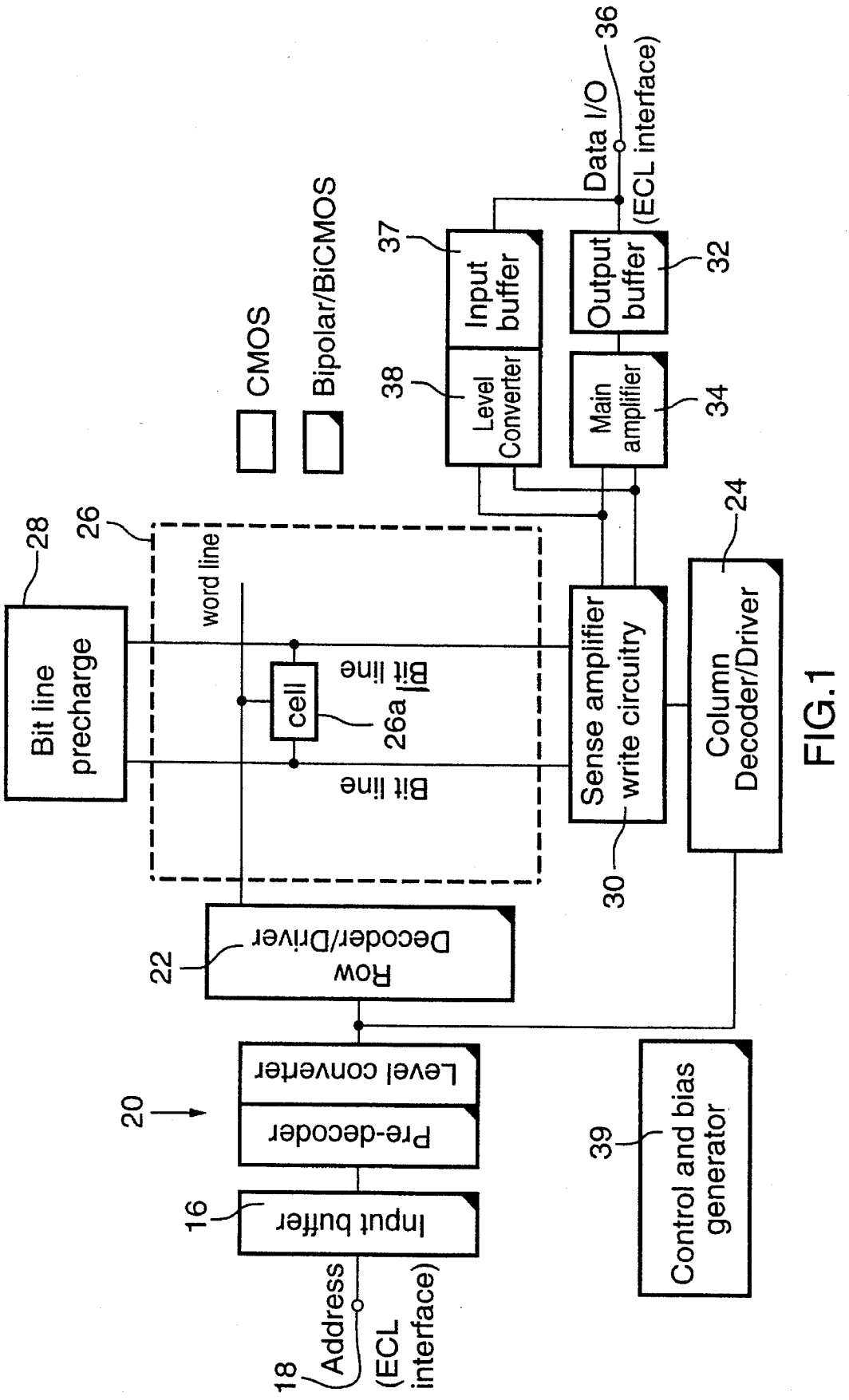

CMOS
Bipolar/BiCMOS
Data I/O
36
(ECL interface)
37
Input buffer
Output buffer
32
38
Level Converter
Main amplifier
34
28
26
word line
24
Bit line precharge
cell
26a
Bit line
Bit line
Sense amplifier write circuitry
Column Decoder/Driver
30
22
Row Decoder/Driver
20
Level converter
Pre-decoder
16
Input buffer
39
Control and bias generator
18
Address
(ECL interface)

FIG.1

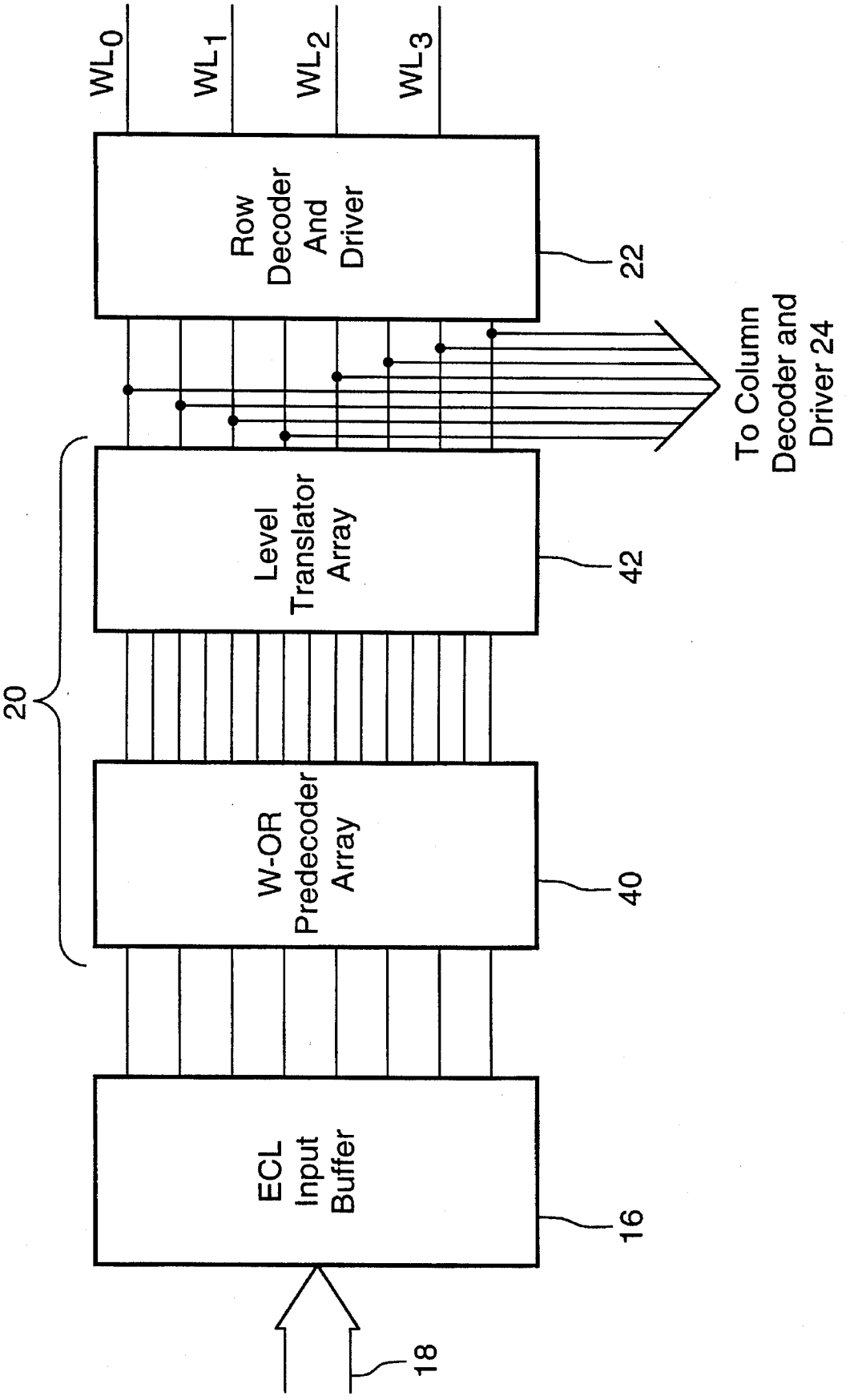

WL0
WL1
WL2
WL3
Row Decoder And Driver
22
To Column Decoder and Driver 24
Level Translator Array
42
20
W-OR Predecoder Array
40
ECL Input Buffer
16
18

FIG.2

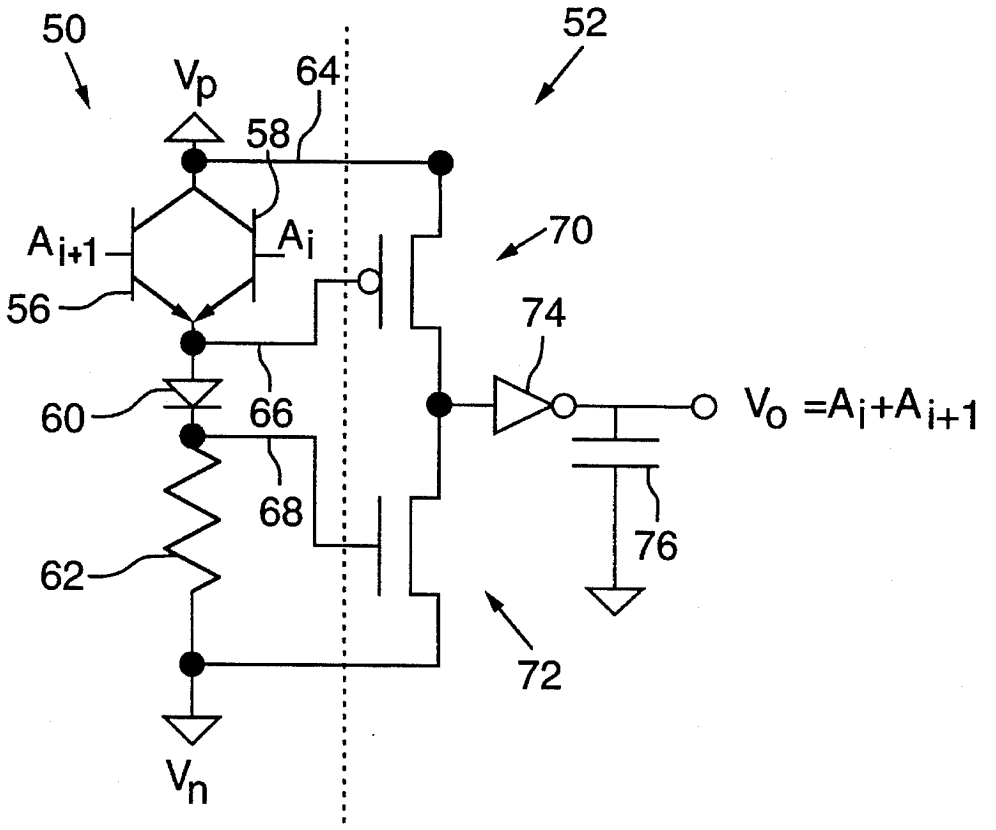


FIG.3

A_i	A_{i+1}	$A_i + A_{i+1}$	$A_i + \overline{A_{i+1}}$	$\overline{A_i} + A_{i+1}$	$\overline{A_i} + \overline{A_{i+1}}$
L	L	L	H	H	H
L	H	H	L	H	H
H	L	H	H	L	H
H	H	H	H	H	L

L=LOW H=HIGH

FIG.4

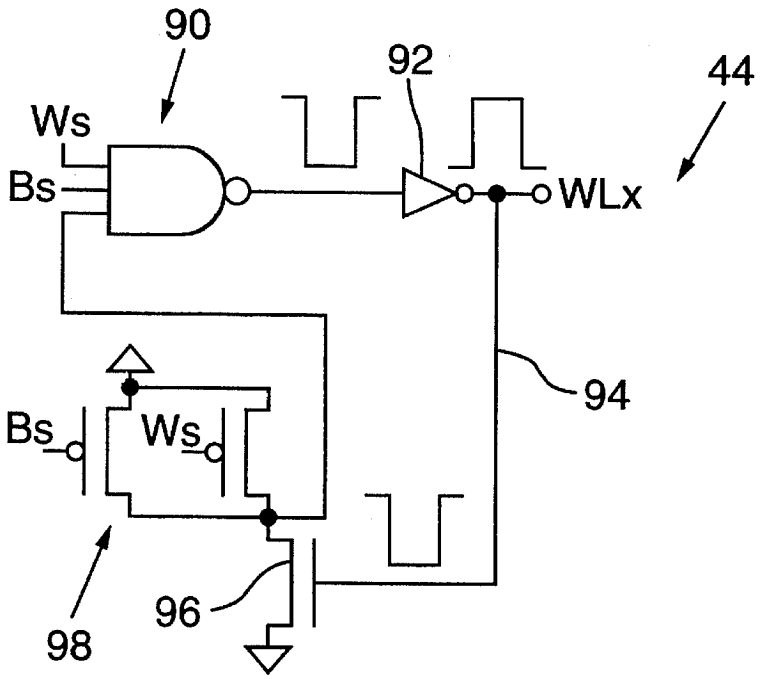

90
92
44
Ws
Bs
WLx
94
Bs
Ws
96
98

FIG.5

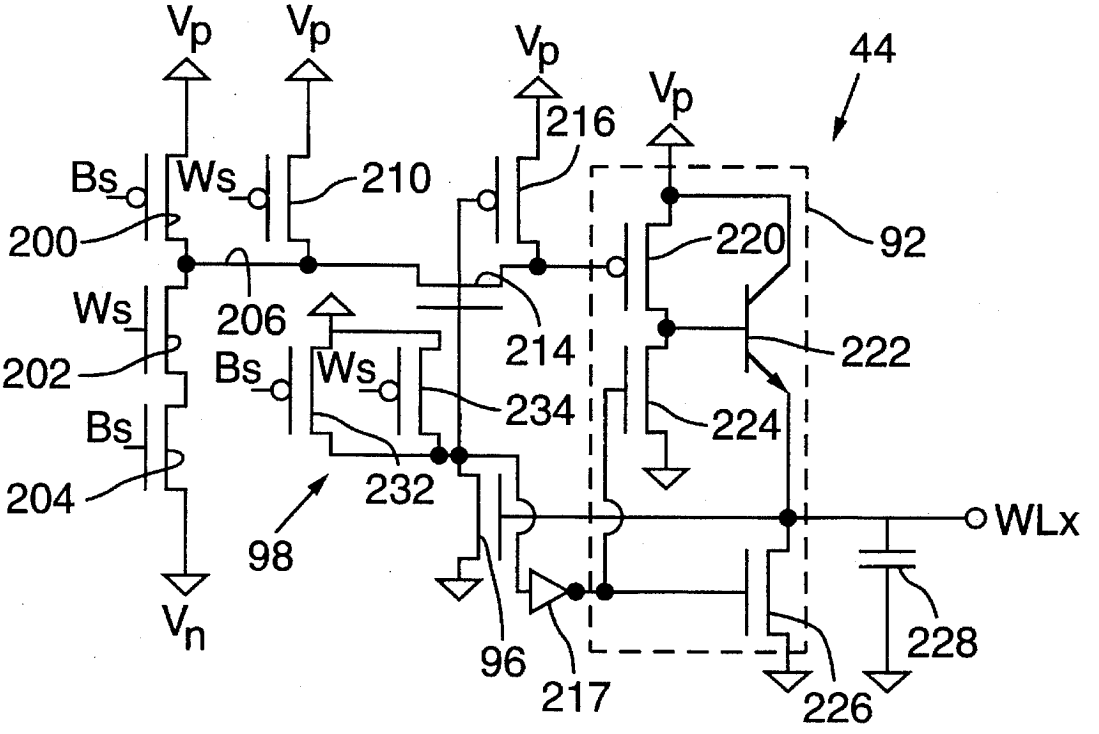

Vp
Vp
Vp
Vp
44
216
Bs
Ws
210
200
220
92
Ws
206
214
222
202
Bs
Ws
234
224
Bs
232
204
98
WLx
Vn
96
217
226
228

FIG.6

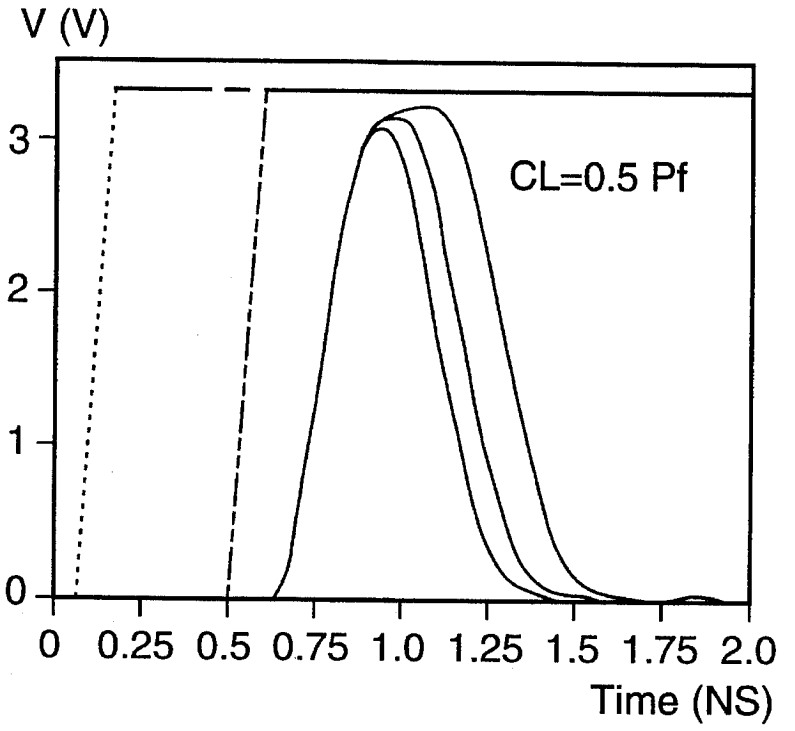

V (V)
3
2
1
0
CL=0.5 Pf
0 0.25 0.5 0.75 1.0 1.25 1.5 1.75 2.0
Time (NS)

FIG.7A

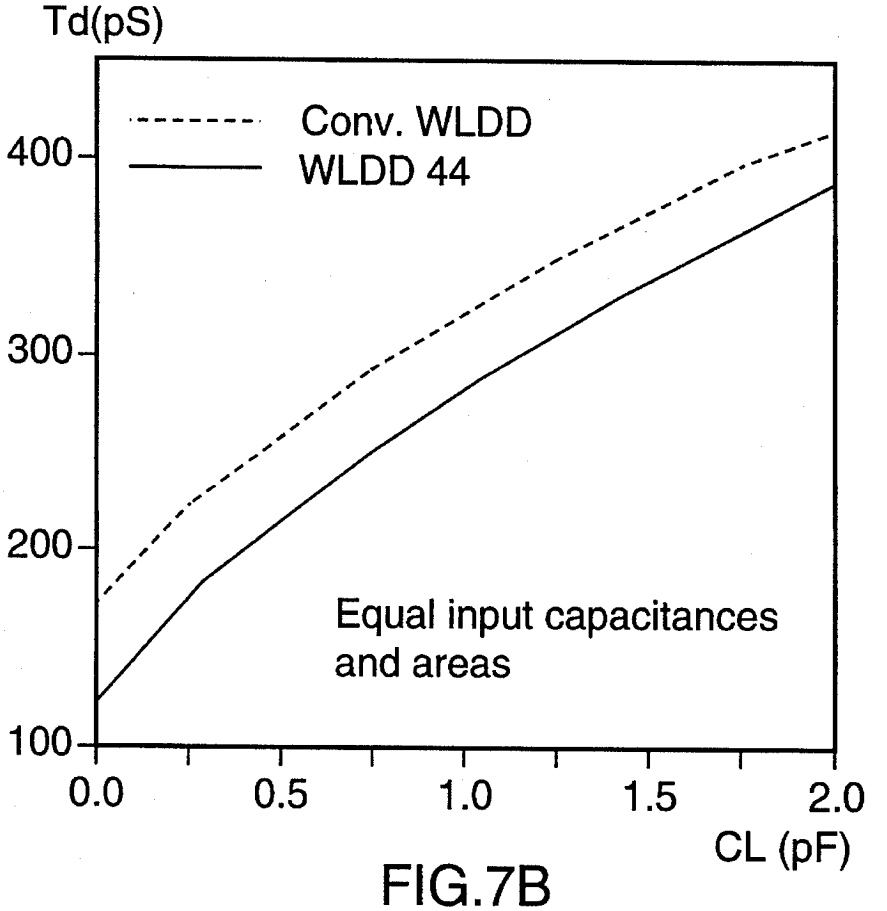

Td(pS)
Conv. WLDD
WLDD 44
400
300
200
100
Equal input capacitances
and areas
0.0 0.5 1.0 1.5 2.0
CL (pF)

FIG.7B

$$Ise\ R2 = \frac{1}{2} Iss\ R1$$

$$\therefore Ise\ R2 = \frac{1}{2}\frac{R1}{R2} Iss \quad or \quad R2 = \frac{1}{2}\frac{Iss}{Ise} R1$$

$$a = \frac{Iss}{Ise}$$

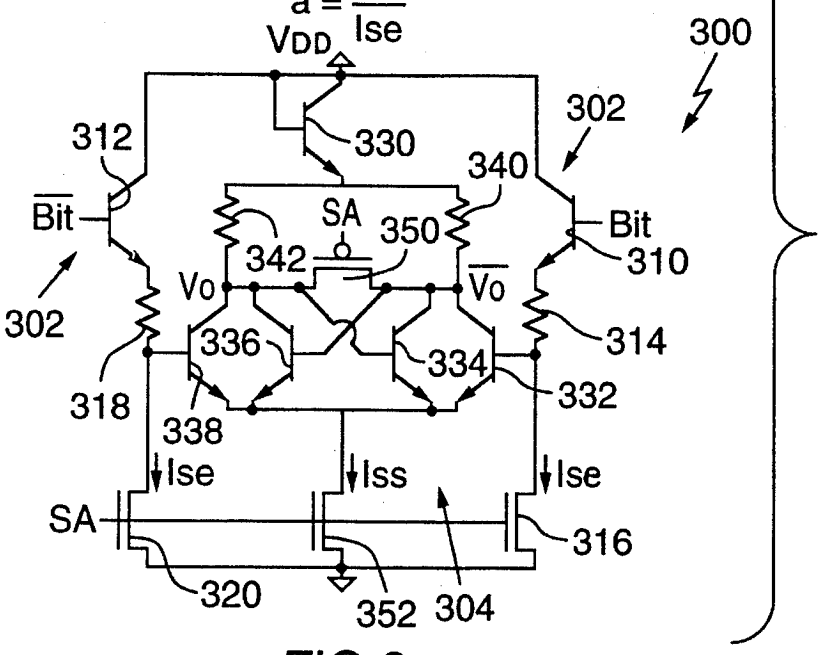


FIG.8

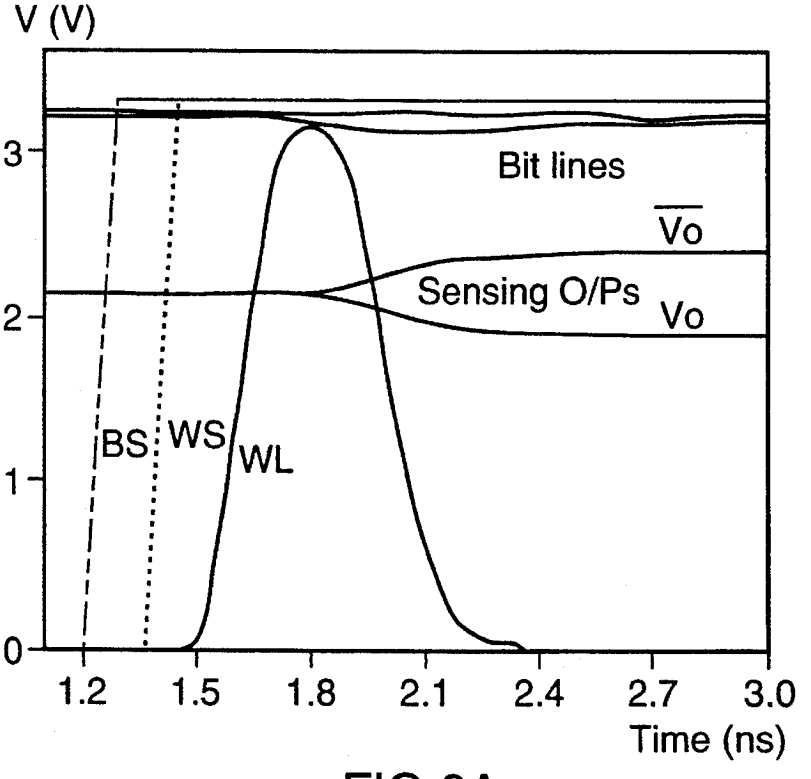


FIG.9A