W-OR predecoder receiving address inputs from said ECL input buffer and generating logic output in response thereto; and a level translator in the form of a single source follower responsive to said W-OR predecoder for level shifting the logic output of said W-OR predecoder;

self-resetting row decoder and driver circuits responsive to said logic OR output values for generating logic word line output pulses to said memory cell array to activate selected cells of said memory cell array corresponding to said address values received by said ECL input buffer;

an unclocked latched ECL sense amplifier array connected to bit lines extending to said memory cell array for sensing the data value of memory cells of said memory cell array activated by said word line output pulses;

column decoder and driver circuits responsive to said logic OR output values to activate the sense amplifiers connected to the selected memory cells; and

an output buffer, coupled to said ECL sense amplifier array, for storing the sensed data values of said selected memory cells.

30. A static random access memory as defined in claim **29** wherein each row decoder and driver circuit includes a logic gate responsive to memory block select and word select inputs from said W-OR predecoder and level translator array and generating said logic word line output pulses in response thereto; a driver responsive to said memory block select and word select inputs and supplying input to said logic gate; and reset means responsive to a logic high word line output pulse and returning the output of said row decoder and driver circuit to a logic low condition after a pre-determined desired duration.

31. A static random access memory as defined in claim **30** wherein said logic high word line output pulses have a pre-determined duration equal to approximately 0.6 nS.

32. A static random access memory as defined in claim **29** wherein each sense amplifier includes an emitter-follower input stage receiving input from complementary bit lines connected to an activated memory cell to be sensed; and an ECL amplifier responsive to said emitter-follower input stage and to memory cell activation signals, said ECL amplifier having latched outputs and generating output signals V_0 and $\overline{V_0}$ thereon representing the sensed state of said memory cell and the complement thereof.

33. A static random access memory as defined in claim **32** wherein each of said sense amplifiers is electrically symmetrical.

34. A static random access memory comprising:

a memory cell array for storing data;

an ECL input buffer receiving address values from an address bus representing memory cell locations in said memory cell array and outputting said address values and complements thereof;

a W-OR predecoder and level translator array connected to said ECL input buffer and receiving said address values and address value complements, said W-OR predecoder and level translator array generating logic OR output values in response to input from said ECL input buffer at MOS signal levels;

self-resetting row decoder and driver circuits responsive to said logic OR output values for generating logic word line output pulses to said memory cell array to activate selected cells of said memory cell array corresponding to said address values received by said ECL input buffer, each row decoder and driver circuit including a logic gate responsive to memory block select and word select inputs from said W-OR predecoder and level translator array and generating said logic word line output pulses in response thereto; a driver responsive to said memory block select and word select inputs and supplying input to said logic gate; and reset means responsive to a logic high word line output pulse and returning the output of said row decoder and driver circuit to a logic low condition after a predetermined duration;

a sense amplifier array connected to bit lines extending to said memory cell array for sensing the data value of memory cells of said memory cell array activated by said word line output pulses, each sense amplifier including an emitter-follower input stage receiving input from complementary bit lines connected to an activated memory cell to be sensed; and an ECL amplifier responsive to said emitter-follower input stage and to memory cell activation signals, said sense amplifier having latched outputs and generating output signals V_0 and $\overline{V_0}$ thereon representing the sensed state of said memory cell and the complement thereof;

column decoder and driver circuits responsive to said logic OR output values and generating said activation signals to activate the sense amplifiers connected to the selected memory cells; and

an output buffer, coupled to said sense amplifier array, for storing the sensed data values of said selected memory cells.

35. A static random access memory as defined in claim **34** wherein said word line output pulses have a predetermined duration equal to approximately 0.6 nS.

36. A static random access memory as defined in claim **35** wherein each of said sense amplifiers is electrically symmetrical.

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