11. A W-OR predecoder and level translation circuit as defined in claim **10** wherein said level translator includes a second pair of FETs, one of said FETs having a drain terminal connected to said output line, a gate terminal connected to a drive line and a source terminal connected to an output node, the other of said FETs having a drain terminal connected to said output node, a gate terminal connected to a drive circuit receiving input from said drive line and a source terminal connected to said low potential node, said FETs being configured so that only one of said FETs is in an on-state at a time.

12. A W-OR predecoder and level translation circuit as defined in claim **11** wherein said one FET is in said on-state when said address inputs to said W-OR predecoder are low to couple said output node to said output line, said level translator further including an inverter having an input terminal connected to the source terminal of said one FET and to the drain terminal of said other FET and having an output terminal leading to said output node.

13. A W-OR predecoder and level translation circuit as defined in claim **12** wherein said drive circuit includes a transistor having a base connected to said drive line, a collector connected to said output line and an emitter connected to the gate of said other FET, said drive circuit further including a third FET and a resistor arranged in parallel between the emitter of said transistor and said low potential node, said third FET having its drain terminal connected to said emitter, its source terminal connected to said low potential node and its gate terminal connected to a feedback path extending from said output node.

14. A row decoder and driver circuit for a static random access memory comprising:

a logic gate responsive to memory block select and word select inputs and generating logic output on an output node in accordance with inputs thereto;

a driver responsive to said memory block select and word select inputs and supplying input to said logic gate; and

reset means responsive to a logic high condition on said output node for returning said output node to a logic low condition after a predetermined duration.

15. A row decoder and driver circuit as defined in claim **14** wherein said reset means includes a semiconductor switch to couple the output node to a low potential terminal to allow said output node to discharge and thereby return said output node to said logic low condition.

16. A row decoder and driver circuit as defined in claim **15** wherein said reset means further includes an inverter responsive to input from said driver, said semiconductor switch being responsive to logic high input from said inverter to couple said output node to said low potential terminal.

17. A row decoder and driver circuit as defined in claim **16** wherein said reset means further includes a second semiconductor switch coupled to said output node via a feedback path, said second semiconductor switch being responsive to said logic high condition on said output node to couple the input terminal of said inverter to said low potential terminal.

18. A row decoder and driver circuit as defined in claim **17** wherein said logic gate is a NAND gate and wherein said driver is a BiCMOS driver.

19. A row decoder and driver circuit as defined in claim **17** wherein the widths of said inverter and said second semiconductor switch are selected to establish said pre-determined duration.

20. A row decoder and driver circuit as defined in claim **19** wherein said widths are selected so that said logic high condition has a pre-determined duration equal to approximately 0.6 nS.

21. A sense amplifier to sense the state of a memory cell in a memory cell array forming a part of a static random access memory comprising:

an emitter-follower input stage receiving input from complementary bit lines connected to an activated memory cell to be sensed; and

an ECL amplifier responsive to said emitter-follower input stage and to memory cell activation signals, said ECL amplifier having latched outputs and generating output signals V_0 and $\overline{V_0}$ thereon representing the sensed state of said memory cell and the complement thereof.

22. A sense amplifier as defined in claim **21** wherein said ECL amplifier maintains said output signals V_0 and $\overline{V_0}$ until said activation signal changes from a logic high state to a logic low state.

23. A sense amplifier as defined in claim **22** wherein said sense amplifier is electrically symmetrical.

24. A sense amplifier as defined in claim **23** wherein said ECL amplifier includes a pair of electrically parallel branches, each branch including a pair of transistors having coupled collectors and emitters, the coupled collectors of said pairs of transistors constituting complementary output nodes on which said output signals V_0 and $\overline{V_0}$ are applied, the base of one transistor of each pair being biased by an emitter follower of said emitter follower input stage, the base of the other transistor of each pair being coupled to the collectors of the other pair of transistors.

25. A sense amplifier as defined in claim **24** wherein said branches are coupled to a high potential node through a diode and are coupled to a low potential node through a first current source responsive to said activation signal.

26. A sense amplifier as defined in claim **25** further including a semiconductor switch interconnecting the collectors of each pair of transistors, said semiconductor switch being responsive to the absence of said activation signal to couple electrically the collectors of each pair of transistors to reset the output on said complementary output nodes.

27. A sense amplifier as defined in claim **26** wherein each of said emitter followers includes a transistor having a collector coupled to said high potential node, a base coupled to one of said complimentary bit lines, and an emitter coupled to the base of a transistor in said ECL amplifier by way of a resistor and coupled to the low potential node by way of said resistor and a second current source, said second current source being responsive to said activation signal.

28. A sense amplifier as defined in claim **27** wherein the resistors in said emitter followers are selected so that the voltage supplied to the base of the transistor in said ECL amplifier is slightly below the voltage at said complimentary output nodes prior to sensing of said memory cell.

29. A static random access memory comprising:

a memory cell array for storing data;

an ECL input buffer receiving address values from an address bus representing memory cell locations in said memory cell array and outputting said address values and complements thereof;

a W-OR predecoder and level translator array connected to said ECL input buffer and receiving said address values and address value complements, said W-OR predecoder and level translator array generating logic OR output values in response to input from said ECL input buffer at MOS signal levels, each W-OR predecoder and level translator in said array including a