translator **152** is achieved by the transistor **175** and the feedback controlled FET **177**. The resistor **179** ensures that the input to the FET **172** is level shifted even when FET **177** is off for a long time. Although the design of this level translator **152** consumes more power than that of the embodiment shown in FIG. **3**, the W-OR predecoder **150** consumes significantly less power than that consumed by W-OR predecoder **50**.

FIG. **12** shows a plot of the power consumption of the W-OR predecoders and level translators shown in FIGS. **3**, **10** and **11**. In each case, the average power of the W-OR predecoder including the ECL input buffer was varied and the level translator was sized to obtain a delay of 600 pS. As can be seen, in the W-OR predecoders and level translators shown in FIGS. **3** and **11**, the power consumption of the W-OR predecoders could not be reduced below 9 mW. The conventional W-OR predecoder and level translator had an optimum power of 15.6 mW. The W-OR predecoder and level translators of FIGS. **3** and **11** however, had optimum powers of 11.7 mW and 10.1 mW respectively.

Although W-OR predecoder **150** and level translator **152** consume less power than those of the embodiment illustrated in FIG. **3**, they also require more area. Therefore, if area constants are critical, W-OR predecoder **50** and level translator **52** are better suited although they consume more power.

By comparing alternative configurations of front-ends for the SRAM **20**, it has been found that an optimum front-end combination for a 16 Mb^+ SRAM access path includes an ECL input buffer, followed by a W-OR predecoder array, immediately followed by a level-translator array and, then followed by BiNMOS word line decoders and drivers. The present SRAM includes such an optimum front-end. The design of the circuits forming the front-end have also been selected to reduce power consumption allowing a SRAM to be developed which significantly reduces overall power consumption as compared to prior art designs. Moreover, the SRAM includes a novel sense amplifier design to reduce further power consumption.

Although specific embodiments of circuit designs for use in a SRAM have been described, those of skill in the art will appreciate that modifications and/or variations may be made to the present invention without departing from the scope thereof as defined by the appended claims.

We claim:

1. A front-end for a static random access memory having a memory cell array for storing data comprising:

an ECL input buffer receiving address values from an address bus representing memory cell locations in said memory cell array and outputting said address values and complements thereof;

a W-OR predecoder and level translator array connected to said ECL input buffer and receiving said address values and address value complements, said W-OR predecoder and level translator array generating logic OR output values in response to input from said ECL input buffer at MOS signal levels, the level translators in said array being in the form of single source followers connected directly to W-OR predecoders; and

self-resetting row decoder and driver circuits responsive to said logic OR output values for generating logic word line output pulses to said memory cell array to activate selected memory cells of said memory cell array corresponding to said address values.

2. A front-end for a static random access memory as defined in claim **1** wherein said row decoder and driver circuits are configured to generate word line output pulses having pulse widths of a desired duration.

3. A front-end for a static random access memory as defined in claim **2** wherein said word line output pulses have pulse widths approximately equal to 0.6 nS.

4. A front-end for a static random access memory as defined in claim **2** wherein said row decoder and driver circuits each include a logic gate responsive to memory block select and word select inputs from said W-OR predecoder and level translator array and generating said word line output pulses in response thereto; a driver responsive to said memory block select and word select inputs and supplying input to said logic gate; and reset means responsive to a logic high word line output pulse and returning the output of said row decoder and driver circuit to a logic low condition after said desired duration.

5. A W-OR predecoder and level translation circuit for the front-end of a static random access memory comprising:

a W-OR predecoder receiving address inputs from an ECL input buffer and generating logic output in response thereto; and

a level translator in the form of a single source follower responsive to said W-OR predecoder for level shifting the logic output of said W-OR predecoder.

6. A W-OR predecoder and level translation circuit as defined in claim **5** wherein said W-OR predecoder includes a pair of transistors having coupled collectors and emitters, each transistor receiving an address input on the base thereof, said collectors being coupled to a high potential node; and a pull-down circuit coupled between said emitters and a low potential node, said W-OR predecoder providing said logic output on an output line coupled to said high potential node and providing drive input to said level translator via at least one drive line coupled to said emitters.

7. A W-OR predecoder and level translation circuit as defined in claim **6** wherein said pull-down circuit includes a diode having one terminal thereof connected to said emitters and a resistor connected between the other terminal of said diode and said low potential node, said W-OR predecoder supplying drive input to said level translator via a pair of drive lines, one of said drive lines being connected to said emitters and the other of said drive lines being connected to the other terminal of said diode.

8. A W-OR predecoder and level translation circuit as defined in claim **7** wherein said level translator includes a pair of FETs, one of said FETs having a drain terminal connected to said output line, a gate terminal connected to said one drive line and a source terminal connected to an output node, the other of said FETs having a drain terminal connected to said output node, a gate terminal connected to said other drive line and a source terminal connected to said low potential node, said FETs being configured so that only one of said FETs is in an on-state at a time.

9. A W-OR predecoder and level translation circuit as defined in claim **8** wherein said one FET is in said on-state when said address inputs to said W-OR predecoder are low to couple said output node to said output line, said level translator further including an inverter having an input terminal connected to the source terminal of said one FET and to the drain terminal of said other FET and having an output terminal leading to said output node.

10. A W-OR predecoder and level translation circuit as defined in claim **6** wherein said pull-down circuit includes a first pair of FETs coupled between said emitters and said low potential node, one of said FETs having a drain terminal connected to said emitters and a source terminal connected to a drain terminal of the other FET, said other FET having a source terminal connected to said low potential node, the gate terminals of each FET receiving a complement of one of the address inputs supplied to said transistors.