tion to the sensed outputs was less than 400 pS for a load of 3 fF at the sensed outputs. Another advantage of this sensing scheme is that the outputs are already level-shifted by the diode-connected transistor **330**.

The design of the sense amplifier **300** makes it very resilient to process and supply variations. This is due to its symmetrical nature, the excellent matching of the bipolar devices, and the fact that resistors **314** and **318**, and the three NMOS current sources (FETs **316**, **320** and **352**) are multiples of one another. Assuming that the resistors **314** and **318** are physically placed adjacent one another, any variation in the values of the resistors due to process variations will be consistent for both resistors. The same applies to the three NMOS FET current sources. Hence equations (1) through (6) will more or less always hold, and process supply variations will have a lesser effect on the correct operation of the sense amplifiers **300** in the array.

One concern with the sense amplifier **300** is the possibility of sensing, amplifying, and latching-in false bit line data (i.e. glitches). The regenerative nature of the sense amplifier **300** makes it prone to such erroneous behavior. To inhibit this from happening, the regenerative effect is slightly delayed, such that any bit line glitch that has a duration less than a certain value will not be latched-in. This is achieved by adjusting resistors **314** and **318**, such that the initial value of the output voltage V_0 (given by equation (1) is slightly below the initial value of the voltages supplied to the bases of transistors **332** and **338** given by equation (2). This results in the following condition prevailing:

$$Vo(t=0^+)=\overline{Vo}(t=^+)=V1(t=0^+)-\Delta V_r=V2(t=0^+)-\Delta V_r \quad (7)$$

Hence the output regeneration will not start until one of the output voltages V_0 and $\overline{V_0}$ rises by at least ΔV_r. The larger the voltage ΔV_r, the more resistant the sense amplifier is to glitches. However, delaying the output regeneration reduces the speed of the sense amplifier **300** and hence, voltage ΔV_r should be kept to a minimum.

FIG. **9***b* shows the effect of bit line glitches on the sense amplifier outputs. Two bit line glitches having a 50 mV amplitude and 100 pS and 200 pS durations respectively, were applied to the sense amplifier **300** inputs. For these results, the sense amplifier **300** was designed such that ΔV_r was about 100 mV. As FIG. **9***b* shows, the temporary disturbance at the outputs were not latched-in. Although the gain of the amplifier was around **20**, the output signals did not reach an amplitude of more than 80 mV before they quickly faded away. The response of the sense amplifier **300** to a correct bit line signal having a 75 mV amplitude and a duration of 500 pS is also shown in FIG. **9***b*. The sense amplifier correctly read the bit line signal and latched it in.

FIG. **9***c* shows the delay versus average power consumed for the sense amplifier **300** and for a conventional ECL sense amplifier having cross-coupled PMOS loads. The optimum delay of sense amplifier **300** was 160 pS, 25% faster than the conventional amplifier. At an average power of 8 mW, sense amplifier **300** had a delay of 250 pS, 20% lower than the conventional amplifier. Although the delay savings of the sense amplifier **300** do not seem significant as compared to the total access time of the SRAM **20**, the power savings from the sensing technique are significant. The sense amplifier **300** also requires less area than the conventional sense amplifier.

Referring now to FIG. **11**, an alternative embodiment of a W-OR predecoder **150** and level translator **152** is shown. In this embodiment like reference numerals of FIG. **3** will be used to indicate like components with a "100" added for clarity. The W-OR predecoder **150** includes a pair of transistors **156** and **158**. The collectors of the transistors **156** and **158** are coupled and lead to a positive voltage source V_p. The base of transistor **158** is connected to the bit $\overline{A_i}$ output of the ECL input buffer **22** and the base of transistor **156** is connected to the bit A_{i+1} output of the ECL input buffer **22**. The emitters of the transistors **156** and **158** are also coupled and lead to the drain of an NMOS FET **159**. The base of FET receives the bit A_i output of the ECL input buffer **22**. The source of FET **159** is connected to the drain of an NMOS FET **161**. The base of FET **161** receives the bit $\overline{A_{i+1}}$ output of the ECL input buffer **22**. The source of FET **161** is connected to ground V_n. The W-OR predecoder **150** also includes a logic output line **164** and a drive line **166** leading from the drain of FET **159**.

The level translator **152** is also in the form of a single source follower. Specifically level translator includes a PMOS FET **170** having its drain connected to output line **164**. The base of FET **170** is connected to the drive line **166**. The source of FET **170** is connected to an inverter **174** as well as to the drain of an NMOS FET **172**. FET **172** has its source connected to ground V_n and its gate connected to the emitter of a transistor **175**. The emitter of transistor **175** is also connected to the drain of an NMOS FET **177** and to one terminal of a large value resistor **179**. The other terminal of the resistor **179** and the source of the FET **177** are connected to ground V_n. Transistor **175** has its collector connected to the output line **164** and its base connected to the drive line **166**. A capacitor **176** has one terminal connected between the inverter **174** and the output node V_o of the level translator **152** and another terminal connected to ground V_n. A feedback line **181** is connected between inverter **174** and capacitor **176** and leads to the gate of FET **177**.

In operation, when the inputs A_i and A_{i+1} are both low, the two transistors **156** and **158** are off and the potential on output line **164** is high and equal to voltage source V_p. The inputs to the gates of FETs **159** and **161** are high thereby coupling drive line **166** to the ground resulting in a logic low being supplied to the gate of FET **170** and to the base of transistor **175**. The logic low input to FET **170** turns it on allowing the high potential on output line **164** to be applied to the inverter **174** resulting in a logic low output at node V_o and a logic low applied to FET **177** maintaining it in an off-state. Although a logic low is applied to the base of transistor **175**, resistor **179** maintains the transistor slightly on to maintain the level shifting (i.e. the V_{BE} drop) of the input to FET **172** keeping the power consumption of the level translator low. In this case, the input to FET **172** is still insufficient to turn it on. Since resistor **179** is large, when FET **177** is off very little current is drawn by the resistor.

When either one or both inputs A_i and A_{i+1} are high, either or both of the transistors **156** and **158** are on and one or both of FETs **159** and **161** are off. This results in the drive line **166** being connected to the voltage source V_p through one or both the transistors **156** and **158** causing transistor **175** to turn on and FET **170** to turn off. With transistor **175** turned on, FET **172** is turned on as a result of the potential on output line **164**. With FET **172** on, inverter **174** is coupled to ground through FET **172** resulting in a logic high output at output node V_0. The logic high output is fed back to FET **177** turning it on.

The pull-down circuitry of the W-OR predecoder **150** in this embodiment is implemented using the FETs **159** and **161** which are controlled by outputs $\overline{A_i}$ and A_{i+1} of the ECL input buffer **22** instead of resistors. This pull-down circuit design consumes the least amount of power when the output is high (i.e. when A_i and A_{i+1} are high) since no current flows through the FETs **159** and **161**. The level-shifting of the level