WLDD circuit **44** significantly increases power savings due to the fact that it generates shorter duration output pulses as compared with conventional circuits. Since the WLDD circuit **44** can be configured to generate an output pulse having a pulse width of 0.6 nS, if a word line is activated by such a pulse (compared to a 5 nS pulse generated by a conventional WLDD circuit), the power consumed by the selected block of memory cells in memory cell array **28** is reduced by more than 8 times.

Referring now to FIG. **8**, an unclocked latched-ECL sense amplifier forming part of sense amplifier array **30** is shown and is generally indicated by reference numeral **300**. The amplifier **300** includes an emitter-follower input stage **302** followed by an ECL amplifier **304** with latched outputs.

The emitter-follower input stage includes a pair of transistors **310** and **312** having their collectors coupled to a positive voltage source V_{DD}. The base of transistor **310** receives input from a bit line Bit while the base of transistor **312** receives input from complement bit line $\overline{Bit}$. The bit lines Bit and $\overline{Bit}$ are pre-charged to voltage V_{DD} by the bit line precharge circuit **28**. The emitter of transistor **310** is connected to the ECL amplifier **304** via a resistor **314** as well as to the drain of an NMOS FET **316**. The emitter of transistor **312** is also connected to the ECL amplifier **304** via a resistor **318** as well as to the drain of an NMOS FET **320**.

The ECL amplifier **304** includes a transistor **330** having its collector and base coupled to voltage source V_{DD}. Because the base of transistor **330** is tied to its collector, transistor **330** acts as a diode. The emitter of transistor **330** leads to the collectors of transistors **332**, **334**, **336** and **338** by way of resistors **340** and **342** respectively. The collectors of transistors **332** and **334** are also connected to the drain of a PMOS FET **350**, as well as to the base of transistor **336**. The collectors of transistors **336** and **338** are also connected to the source of the FET **350**, as well as to the base of the transistor **334**. The gate of FET **350** leads to a signal line SA.

As can be seen, the design of the ECL amplifier **304** is electrically symmetrical. Emitter coupled transistors **332** and **334** and resistor **340** form one branch of the ECL amplifier while emitter coupled transistors **336** and **338** and resistor **342** form a second branch of the ECL amplifier **304**.

The emitters of the four transistors **332** to **338** are coupled and lead to the drain of an NMOS FET **352**. The sources of the FETs **316**, **320** and **352** are coupled to ground. The gates of the FETs **316**, **320** and **352** are also coupled and lead to signal line SA. The sense amplifier **300** provides two outputs V_o and $\overline{V_0}$ representing the logic value of the sensed memory cell and its compliment.

When the sense-amplifier is activated by a logic high on signal line SA from the column decoder and driver, and with the bit lines Bit and $\overline{Bit}$ at their precharged state (i.e. @V_{DD}), the outputs of the sense-amplifier are discharged from their initial level ($\cong V_{DD}-V_{BE}$) to:

$$Vo(t=0^+)=\overline{Vo}(t=0^+)=VDD-V_{BE}-\frac{I_{ss}}{2}\cdot R1 \tag{1}$$

where:

I_{SS} is the ECL amplifier tail current; and

R1 is the resistance of resistors **340** and **342**.

In this state, the tail current I_{SS} is equally divided between the two branches of the ECL amplifier **304**. Also, the voltage outputs of the emitter-followers **302** applied to the bases of transistors **332** and **338** are:

$$V1=V2=VDD-V_{BE}-I_{SE}.R2 \tag{2}$$

where:

I_{SE} is the tail current of the emitter-followers; and

R2 is the resistance of resistors **314** and **318**.

During design, a condition is imposed on the sense-amplifier **300** as follows:

$$\frac{I_{ss}}{2}\cdot R1=I_{se}\cdot R2 \tag{3}$$

which can be expressed as:

$$I_{se}=\frac{1}{2}\,I_{ss}\frac{R1}{R2} \tag{4}$$

or

$$R2=\frac{1}{2}\,R2\frac{I_{ss}}{I_{se}} \tag{5}$$

Hence, the base-emitter voltages of transistors **332** and **338** are equal. The size of the diode-connected transistor **330** is proportional to the ratio between the two currents I_{SS} and I_{SE} to ensure the equality of the base voltages of transistors **332** and **338**.

With the sense amplifier activated, when a memory cell **26***a* connected to the bit lines Bit and $\overline{Bit}$ extending to the sense-amplifier is selected, the memory cell pulls the voltage on one of the bit lines down depending on the logic value stored in the memory cell. If the memory cell contains a logic low, the voltage on bit line Bit is pulled down and the voltage on bit line $\overline{Bit}$ remains at V_{DD}. If the memory cell contains a logic high, the voltage on bit line $\overline{Bit}$ is pulled down and the voltage on bit line Bit remains at V_{DD}. In either case, the drop in the voltage on the bit line Bit or $\overline{Bit}$ is such so as not to compromise the content of the memory cell.

When the voltage on one of the bit lines drops, the current in the transistor connected to that bit line (and hence the current in that branch of the ECL amplifier) starts decreasing from its initial value of $\frac{1}{2}*I_{SS}$. Meanwhile, the current through the other branch starts increasing. This imbalance in the currents of the two branches is converted to a small differential voltage at the sense amplifier outputs V_0 and $\overline{V_0}$ respectively. Due to the back-to-back connections between the two outputs through transistors **334** and **336**, a regenerative effect takes place which causes the total tail current to be quickly switched to the branch connected to the bit line with the higher voltage. At the end of this transition, the entire tail current I_{SS} flows into one of the two transistors **334** or **336**. The sensed output voltages V_0 and $\overline{V_0}$ remain constant even if the bit line voltages change (the latched-in state) until the sense amplifier **300** is reset as a result of the signal on signal line SA becoming low. The voltage difference between the two sensed outputs is:

$$\Delta Vo=I_{SS}.R1 \tag{6}$$

with the high output voltage being equal to $V_{DD}-V_{BE}$. At the end of the memory cell access, the memory cell recharges itself to its pre-sensed logic value.

FIG. **9***a* shows a complete column-sensing operation performed by sense amplifier **300**. This figure shows the block select line and word select line inputs B_S and W_S respectively to a WLDD circuit **44**, the WL, output of the WLDD circuit, the bit line Bit input to the sense amplifier **300** as well as the sensed outputs V_0 and $\overline{V_0}$ of the sense amplifier. The latched sense amplifier **300** correctly read and latched-in the data on the bit lines which were activated for only 0.6 nS by the WLDD circuit **44**. The sense amplifier **300** took less than 100 pS to latch-in the data on the bit lines. When operated at its maximum speed (optimum I_{SS}), the sense amplifier consumes approximately 11 mW of power. At this optimum speed, the total delay from the WL activa-