translator **52** is in the form of a single source follower, the W-OR predecoder **50** and level translator **52** consume less power than conventional W-OR predecoders **550** and level translators **552** such as those shown in FIG. **10**. As can be seen, the conventional W-OR predecoder **550** has a resistor pull-down circuit while the level translator **552** is in the form of a source follower having an NMOS current mirror load.

Referring now to FIG. **5**, one of the word-line decoder and driver (WLDD) circuits **44** forming part of the row decoder and driver **22** in accordance with the present invention is shown. The WLDD circuit **44** includes a NAND gate **90** having memory block select line $B_S$ and word select line $W_S$ inputs. The output of NAND gate **90** leads to an inverter **92** which provides the output of WLDD circuit **44**. A feedback path **94** from the inverter output leads to an NMOS FET **96** forming part of a reset circuit which in turn is connected to a BiNMOS driver **98**. The BiNMOS driver **98** also receives block select line $B_S$ and word select line $W_S$ inputs and supplies its output to NAND gate **90**.

The equivalent circuit diagram of WLDD circuit **44** is shown in FIG. **6**. As can be seen, NAND gate **90** includes PMOS FETs **200**, **210** and **216**, NMOS FETs **202**, **204** and **214** as well as an inverter **217**. Inverter **92** includes PMOS FET **220**, NMOS FETs **224** and **226** as well as a transistor **222**. The specific arrangement of the components forming the WLDD circuit will now be described. In particular, PMOS FET **200** has its drain leading to a positive voltage source $V_p$, its gate connected to a block select line $B_S$ and its source connected to the drain of NMOS FET **202**. The base of FET **202** is connected to a word select line $W_S$ and the source of FET **202** is connected to the drain of NMOS FET **204**. The base of FET **204** is connected to the block select line $B_S$ while the source of FET **204** is connected to ground $V_n$.

A line **206** is connected between the source of FET **200** and the drain of FET **202**. Also connected to the line **206** is the source of PMOS FET **210**. The base of FET **210** is connected to the word select line $W_S$ and the drain of FET **210** is connected to the voltage source $V_p$. The line **206** also leads to the drain of NMOS FET **214** which has its base connected to the BiNMOS driver **98** and to the base of PMOS FET **216**. The source of FET **214** is connected to the source of FET **216**. The drain of FET **216** is connected to the voltage source $V_p$.

PMOS FET **220** has its base connected to the source of FET **216**. The drain of FET **220** is connected to the voltage source $V_p$ and to the collector of transistor **222**. The source of FET **220** is connected to the base of transistor **220** and to the drain of NMOS FET **224**. The source of FET **224** leads to ground while the gate of the FET **224** is connected to the output terminal of the inverter **217**. The output terminal of the inverter **217** is also connected to the gate of NMOS FET **226**. The source of FET **226** is connected to ground while the drain of FET **226** is connected to the emitter of transistor **222**.

A capacitor **228** is coupled between the drain of FET **226** and ground. The gate of FET **96** is coupled between the drain of FET **226** and the emitter of transistor **222**. The source of FET **96** leads to ground while its drain leads to the gates of FETs **214** and **216** and to the sources of PMOS FETs **232** and **234** respectively forming the BiNMOS driver **98**. The drains of FETs **232** and **234** are coupled and lead to the voltage source $V_p$. The gate of FET **232** is connected to the block select line $B_S$ and the gate of FET **234** is connected to the word select line $W_S$.

FETs **200**, **210**, **232**, **234** and **96** and the inverter **217** are designed to have close to minimum widths, since it has been found that they do not have to be large for proper operation of the WLDD circuit **44**. Also, FET **220** and transistor **222** are merged to form a BiPMOS device. These devices have been found to achieve fast full swing operation when turned on and then off during output pull-up transition.

In operation, when one or both of the inputs to the block select and word select lines $B_S$ and $W_S$ respectively, are low FETs **200**, **210**, **232** and **234** are turned on and FETs **202** and **204** remain off. With FETs **232** and **234** turned on, a logic high input is supplied to the gate of FET **214** turning it on. A logic high input is in turn applied to the gate of FET **216** turning it off as well as to the input terminal of inverter **217**. Inverter **217** in turn supplies a logic low output to the gates of FETs **224** and **226** keeping them off. With FET **214** on, the gate of FET **220** is coupled to the voltage source $V_p$ through one or both of FETs **200** and **210** turning it off. The voltage on the gate of FET **220** is greater than or equal to $V_p - V_{tp}$ where $V_{tp}$ is the threshold voltage of the FET. This maintains transistor **222** in an off-state resulting in a logic low appearing on the output node $WL_x$ as well as on the gate of FET **96** keeping it off.

When the inputs on both the block select and word select lines $B_S$ and $W_S$ become high as a result of output received from associated W-OR predecoders and level translators, the gate of FET **220** is discharged through the FETs **214**, **202** and **204** and the FET **220** turns on. As a result, the base of transistor **222** begins charging until the transistor **222** turns on, thereby charging the output node $WL_x$ of the WLDD circuit **44**.

When the output voltage on node $WL_x$ reaches a threshold value, the feedback FET **96** turns on and discharges the gates of FETs **214** and **216**. This causes FET **214** to turn off and FET **216** to turn on. With FET **216** on, the gate of FET **220** becomes coupled to the voltage source $V_p$ through FET **216** causing FET **220** to turn off and inject half of its channel charge into the base of transistor **222**. Transistor **222** in turn conducts further so that the output voltage on node $WL_x$ reaches its full swing. At this point, the input to inverter **217** goes low. Thus, inverter **217** supplies a logic high to FET **226** turning it on so that the voltage on output node $WL_x$ is discharged to ground bringing the output node low once again. Inverter **217** also supplies a logic high to the gate of FET **224** turning it on allowing the base of transistor **222** to discharge to ground and thereby turning transistor **222** off.

By controlling the sizes of the FET **96** and the inverter **217**, the width of the output pulse appearing on output node $WL_x$ can be controlled. FIG. **7***a* shows the output of the WLDD circuit **44** in accordance with the present invention for a number of widths of FET **96** and inverter **217**. As the Figure shows, when the inputs on the block select and word select lines $B_S$ and $W_S$ respectively are high, the WLDD circuit **44** produces a pulse with a finite width that is a function of the feedback speed. As the feedback speed increases, the pulse width becomes smaller. It can also be seen that there is a slight loss of output swing when the feedback speed is made very fast although this loss in swing is insignificant for a pulse width of 600 pS.

The WLDD circuit **44** was compared to a conventional BiNMOS WLDD circuit made up of a two-input CMOS NAND gate followed by a BiNMOS driver. Both circuits were designed to have equal input capacitances and areas. FIG. **7***b* shows the rise delays (from 50 percent of the input to 50 percent of the rising output) of both circuits. As can be seen, the delay of the WLDD circuit **44** is slightly less than that of the conventional circuit.

Although the speed improvement of the WLDD circuit is not large as compared with the conventional circuit, the