by reference numeral **14**. SRAM **14** includes an emitter coupled logic (ECL) address input buffer **16** receiving address input A_i, $A_{1+1} \ldots A_{i+n}$ from an address bus **18**. The ECL input buffer **16** in turn outputs each address value A_x received from the address bus **18** together with its complement $\overline{A_x}$. Receiving the output of the ECL input buffer **16** is address conditioning circuitry **20**. Circuitry **20** provides input to a row decoder and driver **22** as well as to a column decoder and driver **24**. Word-lines (WLs) extend from the row decoder and driver **22** and lead to a memory cell array **26**. Bit lines extend from the memory cell array **26** and lead to a bit line precharge circuit **28** as well as to a sense amplifier array and write circuitry **30**. Each cell **26***a* in the memory cell array **26** is connected to one of the word lines and to consecutive bit lines Bit and $\overline{\text{Bit}}$ respectively. The sense amplifier array and write circuitry **30** is connected to the column decoder and driver **24** as well as to an ECL output buffer **32** by way of an amplifier **34**. The ECL output buffer **32** is also connected to a data bus **36**. A data input buffer **37** is also connected to the data bus **36** as well as to the sense amplifier array and write circuitry **30** by way of a level converter **38**. A control and bias generator **39** is included in the SRAM **14** to control whether data is to be read from or written to the memory cell array **26**.

FIG. **2** better illustrates the address conditioning circuitry **20** and the row decoder and driver **22**. As can be seen, address conditioning circuitry **20** includes an ECL wired-OR (W-OR) predecoder array **40** connected to the ECL input buffer **16** as well as to a level translator array **42**. The level translator array **42** provides block select and word select line inputs to self-resetting word-line decoder and driver (WLDD) circuits **44** (best seen in FIGS. **5** and **6**) constituting the row decoder and driver **22**. The output of the WLDD circuits **44** is applied to the word-lines WL_x leading to the memory cell array **26**. The level translator array **42** also provides input to the column decoder and driver **24**.

In operation, when it is desired to read data from the memory cell array **26** and an address is received by the ECL input buffer **167**, the address information is predecoded and translated before being supplied to the row and column decoder and drivers **22** and **24** respectively. The row decoder and driver uses the address information to select the desired memory cells **26***a* corresponding to the received address information. The column decoder and driver **24** uses the address information to activate the sense amplifiers associated with the selected memory cells **26***a* so that the sense amplifiers can sense the state of the memory cells. The sense amplifiers in turn supply output representing the sensed state of the activated memory cells to the ECL output buffer **32** via amplifier **34**.

When it is desired to write data to the memory cell array **26** and an address is received by the ECL input buffer **16**, a similar process is carried out with the exception that the column decoder and driver **24** activates the write circuitry associated with the selected memory cells **26***a*. The write circuitry receives data to be written to the memory cells **26***a* via input buffer **37** and level converter **38** and writes the data to selected memory cells.

The general operation of SRAM **14** is conventional. However, the design of the SRAM **14** is such to reduce power consumption while maintaining memory cell access speed. In order to reduce power consumption novel circuitry in the W-OR predecoder, level translator and sense amplifier arrays as well as in the WLDD circuits constituting the row decoder and driver **22** has been designed and will now be described.

Referring now to FIG. **3**, an embodiment of a W-OR predecoder **50** and level translator **52** forming part of the arrays **40** and **42** respectively is shown. As can be seen, W-OR predecoder **50** includes a pair of transistors **56** and **58**. The collectors of the transistors **56** and **58** are coupled and lead to a positive voltage source V_p. The base of transistor **58** is connected to the bit A_i output of the ECL input buffer **16** and the base of transistor **56** is connected to the bit A_{i+1} output of the ECL input buffer **16**. The emitters of the transistors **56** and **58** are also coupled and lead to the anode of a diode **60**. The cathode of the diode **60** is connected to ground V_n through a resistor **62**. The diode **60** and resistor **62** form the pull-down circuitry of the W-OR predecoder **50**. The W-OR predecoder **50** also includes a logic output line **64** and two drive lines **66** and **68** respectively.

The level translator **52** is in the form of a single source follower and since it directly follows the W-OR predecoder **50**, no problems arise as a result of using the two drive lines **64** and **66** respectively. Specifically, the level translator **52** includes a PMOS field effect transistor (FET) **70**, an NMOS FET **72**, an inverter **74** and a capacitor **76**. FET **70** has its drain connected to output line **64** and its gate connected to the drive line **64**. The source of FET **70** is connected to the inverter **74** as well as to the drain of FET **72**. FET **72** has its gate connected to the drive line **68** and its source connected to ground V.. The capacitor **76** has one terminal connected between the inverter **74** and the output node V_o of the level translator **52** and another terminal connected to ground V_n. The level translator **52** ensures that the output of the W-OR predecoder **50** is at CMOS levels. The inverter **74** ensures full-signal restoration and functions as a pre-driver for the following word-line decoder and driver circuit **44**.

In operation, when the inputs A_i and A_{i+1} are both low, the two transistors **56** and **58** respectively are off and the potential on output line **64** is high and equal to the voltage source V_p. The potential on drive lines **66** and **68** is low turning FET **70** on and FET **72** off. Thus, the high potential on output line **64** is applied to inverter **74** through FET **70** resulting in a logic low output on output node V_o.

When either one or both inputs A_i and A_{i+1} is high, one or both of the transistors **56** and **58** is on. This results in the drive line **66** becoming coupled to the voltage source V_p through one or both of the transistors placing a high potential on the drive line **66**. This causes FET **70** to turn off. When one or both of the transistors **56** and **58** is on, drive line **68** also becomes coupled to the voltage source V_p through one or both of the transistors as well as through diode **60**. This causes FET **72** to turn on. Therefore, the inverter **74** becomes coupled to ground through FET **72** resulting in a logic high output on output node V_o.

The logic output on output node V_o is supplied to either a block select line or word select line input of one of the WLDD circuits **44**. Therefore, depending on the logic value inputs A_x and A_{x+1} to the various W-OR predecoders **50** in the array **40**, different logic values are supplied to the various block select line and word select line inputs to the WLDD circuits **44**. This allows selected blocks of the memory cell array **28** to be activated.

FIG. **4** shows the output of the W-OR predecoder **50** and level translator **52** under column A_i+A_{i+1} for the various values of logic inputs A_i and A_{i+1}. Since the ECL input buffer **16** generates two address outputs A_x and $\overline{A}$ for each address input A_x, four W-OR predecoders **50** and level translators **52** of the type shown in FIG. **3** are necessary to generate the logic outputs under the four columns of the table illustrated in FIG. **4**.

Because the diode **60** level shifts the input signal to the FET **72** when the FET is turned on and because the level