According to still yet another aspect of the present invention there is provided a sense amplifier to sense the state of a memory cell in a memory cell array forming a part of a static random access memory comprising:

an emitter-follower input stage receiving input from complementary bit lines connected to an activated memory cell to be sensed; and

an ECL amplifier responsive to said emitter-follower input stage and to memory cell activation signals, said ECL amplifier having latched outputs and generating output signals $V_0$ and $\overline{V_0}$ thereon representing the sensed state of said memory cell and the complement thereof.

According to still yet another aspect of the present invention there is provided a static random access memory comprising:

a memory cell array for storing data;

an ECL input buffer receiving address values from an address bus representing memory cell locations in said memory cell array and outputting said address values and complements thereof;

a W-OR predecoder and level translator array connected to said ECL input buffer and receiving said address values and address value complements, said W-OR predecoder and level translator array generating logic OR output values in response to input from said ECL input buffer at MOS signal levels, each W-OR predecoder and level translator in said array including a W-OR predecoder receiving address inputs from said ECL input buffer and generating logic output in response thereto; and a level translator in the form of a single source follower responsive to said W-OR predecoder for level shifting the logic output of said W-OR predecoder;

self-resetting row decoder and driver circuits responsive to said logic OR output for generating logic word line output pulses to said memory cell array to activate selected cells of said memory cell array corresponding to said address values received by said ECL input buffer;

an unclocked latched ECL sense amplifier array connected to bit cells extending to said memory cell array for sensing the data value of memory cells of said memory cell array activated by said word line output pulses;

column decoder and driver circuits responsive to said logic OR output values to activate the sense amplifiers connected to the selected memory cells; and

an output buffer for storing the sensed data values of said selected memory cells.

According to still yet another aspect of the present invention there is provided a static random access memory comprising:

a memory cell array for storing data;

an ECL input buffer receiving address values from an address bus representing memory cell locations in said memory cell array and outputting said address values and complements thereof;

a W-OR predecoder and level translator array connected to said ECL input buffer and receiving said address values and address value complements, said W-OR predecoder and level translator array generating logic OR output values in response to input from said ECL input buffer at MOS signal levels;

self-resetting row decoder and driver circuits responsive to said logic OR output for generating logic word line output pulses to said memory cell array to activate selected cells of said memory cell array corresponding to said address values received by said ECL input buffer, each row decoder and driver circuit of said array including a logic gate responsive to memory block select and word select inputs from said W-OR predecoder and level translator array and generating said logic word line output pulses in response thereto; a driver responsive to said memory block select and word select inputs and supply input to said logic gate; and reset means responsive to a logic high word line output pulses and returning the output of said row decoder and driver circuit to a logic low condition after a pre-determined duration;

a sense amplifier array connected to bit cells extending to said memory cell array for sensing the data value of memory cells of said memory cell array activated by said word line output pulses, each sense amplifier including an emitter-follower input stage receiving input from complementary bit lines connected to an activated memory cell to be sensed; and an ECL amplifier responsive to said emitter-follower input stage and to memory cell activation signals, said ECL amplifier having latched outputs and generating output signals $V_0$ and $\overline{V_0}$ thereon representing the sensed state of said memory cell and the complement thereof;

column decoder and driver circuits responsive to said logic OR output values and generating said activation signals to activate the sense amplifiers connected to the selected memory cells; and

an output buffer for storing the sensed data values of said selected memory cells.

## BRIEF DESCRIPTION OF THE DRAWINGS

Embodiments of the present invention will now be described more fully with reference to the accompanying drawings in which:

FIG. **1** is a schematic of a BiCMOS/ECL SRAM in accordance with the present invention;

FIG. **2** is a schematic of a portion of the SRAM shown in FIG. **1**;

FIG. **3** is a circuit diagram of an embodiment of a W-OR predecoder and level translator forming part of the SRAM shown in FIG. **1**;

FIG. **4** is a logic table of the output of the W-OR predecoder and level translator shown in FIG. **3**;

FIG. **5** is a schematic diagram of an embodiment of a word-line decoder and driver circuit forming part of the SRAM shown in FIG. **1**;

FIG. **6** is a circuit diagram of the word-line decoder and driver circuit shown in FIG. **5**;

FIGS. **7***a* and **7***b* are graphs showing performance characteristics of the word-line decoder and driver circuit shown in FIGS. **5** and **6**;

FIG. **8** is a circuit diagram of an ECL sense amplifier forming part of the SRAM shown in FIG. **1**;

FIGS. **9***a*, **9***b* and **9***c* are graphs showing performance characteristics of the ECL sense amplifier shown in FIG. **8**;

FIG. **10** is a circuit diagram of a prior art W-OR predecoder and level translator;

FIG. **11** is a circuit diagram of another embodiment of a W-OR predecoder and level translator; and

FIG. **12** is a graph showing performance characteristics of the W-OR predecoder and level translators shown in FIGS. **3**, **10** and **11**.

## DESCRIPTION OF THE PREFERRED EMBODIMENTS

Referring now to FIG. **1**, a BiCMOS/ECL static random access memory (SRAM) is shown and is generally indicated