LOW-POWER BICMOS/ECL SRAM

FIELD OF THE INVENTION

The present invention relates to static random access memory (SRAM) and in particular to a low-power BiCMOS/ECL SRAM and novel circuits for use therein.

BACKGROUND OF THE INVENTION

One of the most successful applications of BiCMOS technology has been in the design of static random access memories (SRAMs). By combining the high-density and lower power dissipation of CMOS technology with the extremely fast speed of bipolar emitter coupled logic (ECL) techniques, BiCMOS/ECL SRAMs have achieved speeds very close to those of bipolar SRAMs at power levels close to those of CMOS SRAMs. In the past, BiCMOS/ECL SRAMs were usually designed to operate at a maximum power level allowed by still or forced-air cooled plastic packages, typically in the range of 600 to 1000 milliwatts for maximum speed. With each new generation of BiCMOS/ECL SRAM, the speed of the BiCMOS/ECL SRAM was enhanced by scaling the technology and/or using novel circuit techniques and architectures, while keeping the power consumption at a relatively constant level.

Although the speed of BiCMOS/ECL SRAMs increased steadily with each new generation while maintaining the power consumption basically constant, a problem existed in that less power was allocated to the ECL input/outputs (I/Os) which increased by 2 with each new generation. Hence, the speed advantage of the ECL I/Os decreased with each new generation. Coupled with the fact that it is very difficult to implement automatic address transition detection (ADT) techniques with ECL address inputs in order to reduce power consumption, the development of asynchronous 16 megabyte$^+$ (Mb$^+$) BiCMOS/ECL SRAMs has been hindered.

Typically, the input buffers, predecoders and level translators consume 40 to 60 percent of a BiCMOS/ECL SRAM's total power. Hence, any reduction in the power consumption of these circuits will amount to a considerable savings in the overall power consumption of the BiCMOS/ECL SRAM.

Another source of power consumption in BiCMOS/ECL SRAMs is a result of the DC power drawn by the memory cell array during memory access. All of the columns in a selected memory block of the memory cell array consume DC power as long as one of the word-lines (WL) of the selected memory block is activated. Techniques such as array division, divided word-line (DWL) and hierarchial word decoding (HWD) which are used to reduce decoding delay, also reduce the block size of the memory blocks and hence, DC currents drawn by them when activated. However, there is a limit to the amount of array division that can be done due to area and delay constraints.

For a 16 Mb SRAM that is divided into 64 memory blocks, the number of columns per memory block is 256. This number is sufficiently large to result in a significant DC current being drawn during memory block activation. If each column in the activated memory block draws a 200 μA current, the total active memory block current would be more than 50 mA. Hence, the DC power consumed by the activated memory block is about 15 to 25 percent of the total active power consumption of the BiCMOS/ECL SRAM.

A scheme to reduce word-line activation time of a 0.5 Mb SRAM was discussed in a paper entitled "A 2-nS Cycle, 3.8-nS Access 512 kb CMOS ECL SRAM with a Pipelined Architecture" authored by T. Chappell et al. and published in the IEEE Journal of Solid-State Circuits, Vol. 26 at pages 1577 to 1585, 1991. The architecture disclosed in this article is intended to reduce the cycle time and pipeline the memory access operation. It utilizes self-resetting blocks for clock generation and global X/Y/Z-decoder lines. The architecture requires a very tight timing control over the self-resetting blocks to ensure correct operation of the SRAM. For a 16 Mb$^+$ SRAM, this is more difficult to achieve and would require the output pulses of the self-resetting blocks to be made long enough to ensure proper operation. However, by increasing the length of the output pulses, power consumption increases. Also, the capacitances on the global decoder lines due to the pulsing of the decoder lines would on average increase the dynamic power dissipation of the SRAM. Accordingly, alternative architectures to reduce SRAM power consumption are continually being sought.

It is therefore an object of the present invention to provide a novel BiCMOS/ECL SRAM and novel circuits for use therein.

SUMMARY OF THE INVENTION

According to one aspect of the present invention there is provided a front-end for a static random access memory having a memory cell array for storing data comprising:

an ECL input buffer receiving address values from an address bus representing memory cell locations in said memory cell array and outputting said address values and complements thereof;

a W-OR predecoder and level translator array connected to said ECL input buffer and receiving said address values and address value complements, said W-OR predecoder and level translator array generating logic OR output values in response to input from said ECL input buffer at MOS signal levels, the level translators in said array being in the form of single source followers connected directly to W-OR predecoders; and

self-resetting row decoder and driver circuits responsive to said logic OR output values for generating logic word line output pulses to said memory cell array to activate selected memory cells of said memory cell array corresponding to said address values.

According to another aspect of the present invention there is provided a W-OR predecoder and level translation circuit for the front-end of a static random access memory comprising:

a W-OR predecoder receiving address inputs from an ECL input buffer and generating logic output in response thereto; and

a level translator in the form of a single source follower responsive to said W-OR predecoder for level shifting the logic output of said W-OR predecoder.

According to still yet another aspect of the present invention there is provided a row decoder and driver circuit for a static random access memory comprising:

a logic gate responsive to memory block select and word select inputs and generating logic output on an output node in accordance with inputs thereto;

a driver responsive to said memory block select and word select inputs and supplying input to said logic gate; and

reset means responsive to a logic high condition on said output node for returning said output node to a logic low condition after a predetermined duration.