US005602774A

United States Patent [19]

Elrabaa et al.

[11] Patent Number: 5,602,774

[45] Date of Patent: Feb. 11, 1997

[54] **LOW-POWER BICMOS/ECL SRAM**

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[21] Appl. No.: **558,896**

[22] Filed: **Nov. 16, 1995**

[51] **Int. Cl.**[6] **G11C 11/40**

[52] **U.S. Cl.** **365/177**; 365/189.05; 365/189.11; 365/189.08; 365/190; 365/205; 365/225.6; 365/230.06; 365/230.08

[58] **Field of Search** 365/177, 189.05, 365/189.11, 190, 205, 225.6, 227, 230.06, 230.08, 189.08

[56] **References Cited**

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[57] **ABSTRACT**

A SRAM includes an ECL input buffer connected between an address bus and a W-OR predecoder array. The logic output of the W-OR predecoder array is applied to a level translator array and level shifted. The level shifted output of the level translator array is supplied to a plurality of self-resetting word-line decoder and driver (WLDD) circuits. The WLDD circuits supply activation pulses to selected blocks of memory in a memory cell array. Sense amplifiers sense and latch-in the data stored in the activated selected blocks of memory. The design of the W-OR predecoder array, level translator array, WLDD circuits and sense amplifiers is such to reduce the overall power consumption of the SRAM.

36 Claims, 9 Drawing Sheets