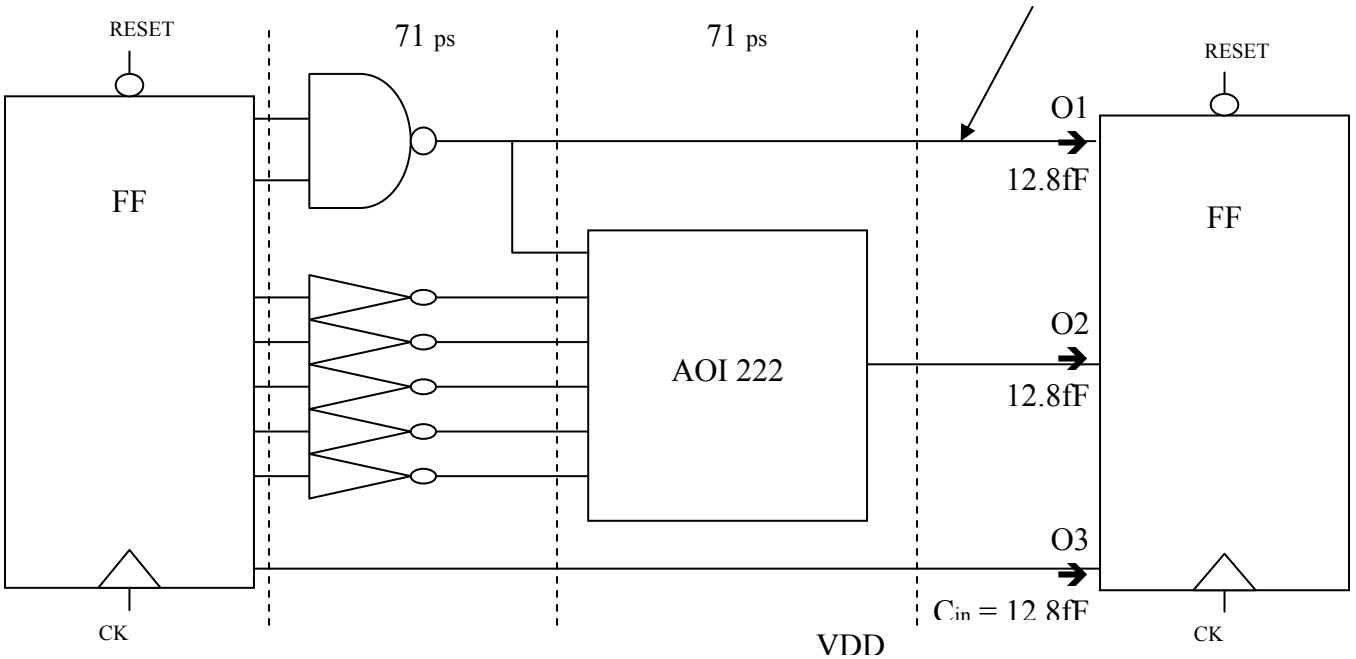
Design of Synchronous Circuit, *continued:*

Example 1: continued

Assume the wire capacitance is C_{W1} =50fF



➔ Start designing the logic
➔ starting from Last level first

The AOI222

$W_{Neff} = W_N/2$

$W_{Peff} = W_p/3$

For Symmetrical NMOS
➔Equal T_f and T_r: $W_{Peff} = 2\ W_{Neff}$

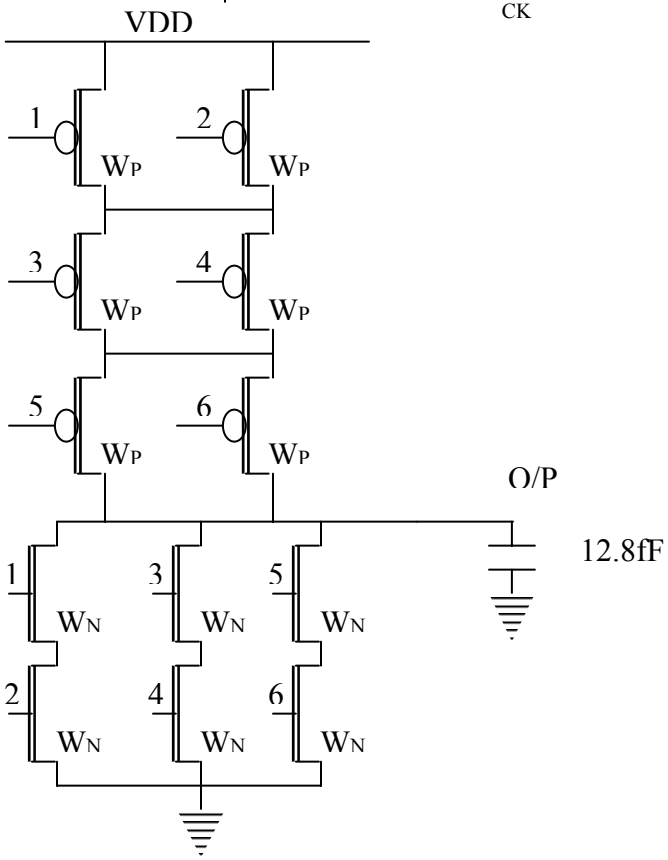
➔ $W_P/3 = 2W_N/2$ ➔ $\boxed{W_P = 3W_N}$

$T_{Dave} = 71$ ps $= T_r = T_f = R_N C_L$

➔ $R_N = 71/12.8 = 5K\Omega$

$W_{Neff} = 4.2/(1000X10^{-6}X5X10^{3}) \approx 0.8$ um

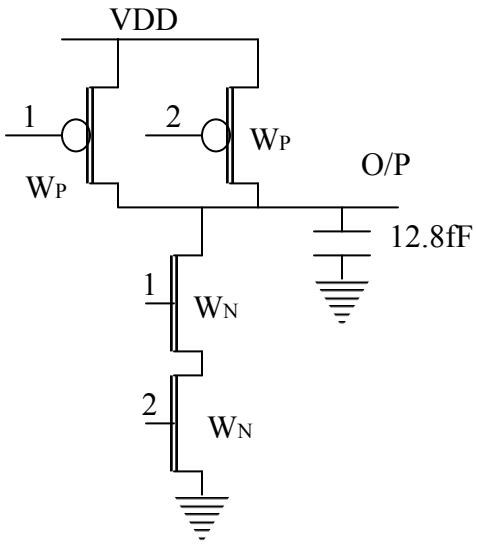
$W_N = 2W_{Neff} = 1.6$ um ➔ $W_P = 4.8$ um



$C_{inAOI222}$ = 2fF X (1.6 + 4.8) = 12.8fF

<u>NAND Gate</u> - AI2: $C_L = C_{W1} + C_{inAOI222} + C_{inFF}$

C_L= 50fF + 12.8fF + 12.8fF = 75.6fF



T_f =71 ps = $R_N C_L$ ➔ R_N =71 ps/75.6fF = 940 Ω

$W_{Neff} = W_N/2$

$W_{Peff} = W_P$

➔ W_{Peff} = ➔ $\boxed{W_P = W_N}$

W_{Neff} =4.2/ ($1000X10^{-6}$ X0.94X10³) ≈ 4.8 um

➔ $W_N = 2W_{Neff}$ = 9.6 um = W_P

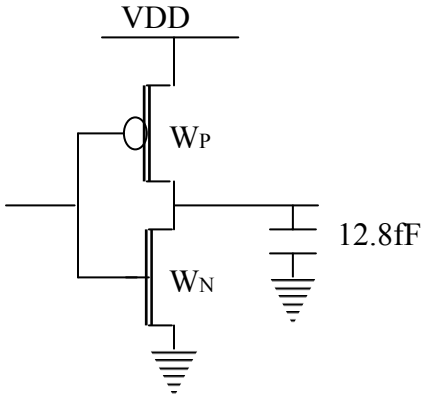
Cin = 2 X 1 X (9.6 + 9.6) = 38fF < 50fF ((assumed CL for FF))

➔ Our FF will work fine

<u>INV1:</u>

$W_{Neff} = W_N$ $W_{Peff} = W_P$

$\boxed{2W_N = W_P}$



R_N =71/12.8 = 6KΩ

W_N= 4.2/ ($1000X10^{-6}$ X 6 X10³) <1 um

So let W_N = 1 um and W_P = 2 um

We have to make sure that the direct connection O3 dose not violate the hold time of the 2nd set of FFs

Our $T_{CK \rightarrow q1}$ = 142 ps assuming load of 50 fF

But for O3, C_L = 12.8fF

$T_{CK \rightarrow q1} = T_{DG1} + T_{Dslave\ logic}$ = 71+71X12.8/50 ≈ 89 ps

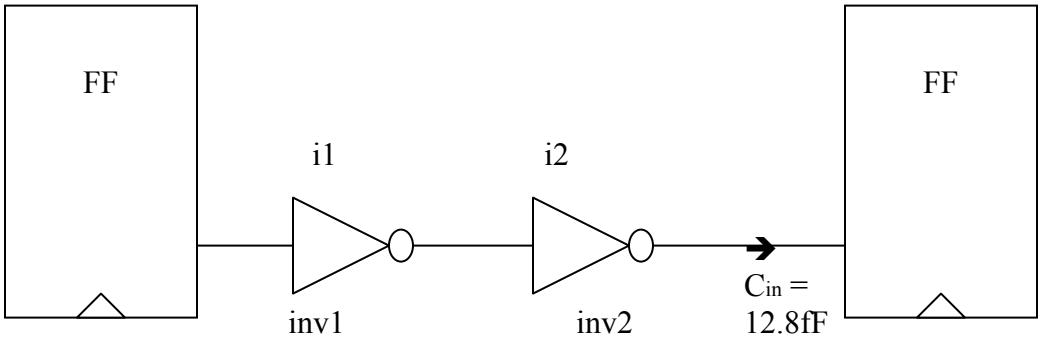
Now assuming that T_{hold}= 100 ps

The condition for satisfying the hold time

$T_{hold} + T_{skew} + T_{jitter} < T_{CK \rightarrow q1} + T_D$

170 ps ≮ 89 ps *VIOLATION!!*

We need to DELAY O3➔use 2 inverters, same one that was designed. And check for both, T_{hold} and T_{SU} violations.



T_{Di2} = 71 ps (it was designed to have T_D = 71 ps at C_L = 12.8fF)

$C_{in\ inv1}$ = 2 X 1 X (2 +1) = 6fF

> For a Designed gate with a delay T_{D1} at load C_{L1}, the new delay T_{D2} for a different load C_{L2} is
>
> $T_{D2} = T_{D1}.C_{L2}/C_{L1}$

➔ T_{Di1} = 71 X 6/12.8 ≈ 30 ps

➔ T_{DO3} = 71 + 30 ≈ 100 ps

Now we check T_{hold} violation:

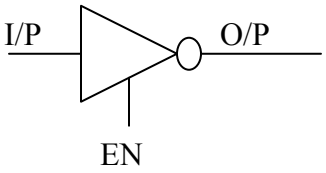
For O3 $T_{CK \rightarrow q1} + T_D$ = 190 ps > $T_{hold} + T_{skew} + T_{jitter}$

Now we check T_{SU} violation:
$T_{CK \rightarrow q1} + T_D + T_{SU}$ = 190 ps + 142 ps = 332 ps < T_{CK}

So no T_{hold} or T_{SU} violations

An Alternative FF Circuits:

Using tri-state Buffers:

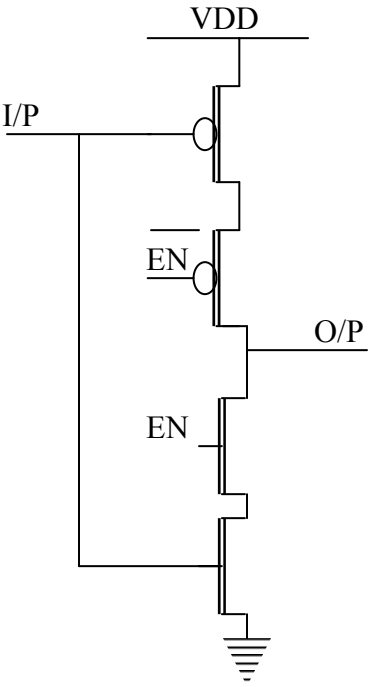


Tri-State Buffer

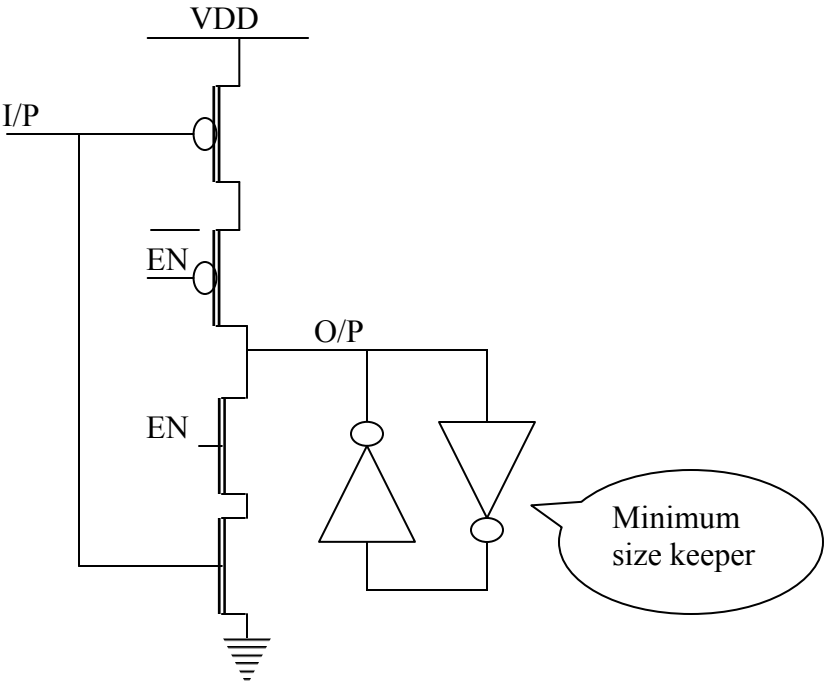
EN	I/P	O/P	
0	X	Z	→ high impedance or open circuit
1	0	1	→ work as inverter when it is enabled
1	1	0	

Used in Buses:

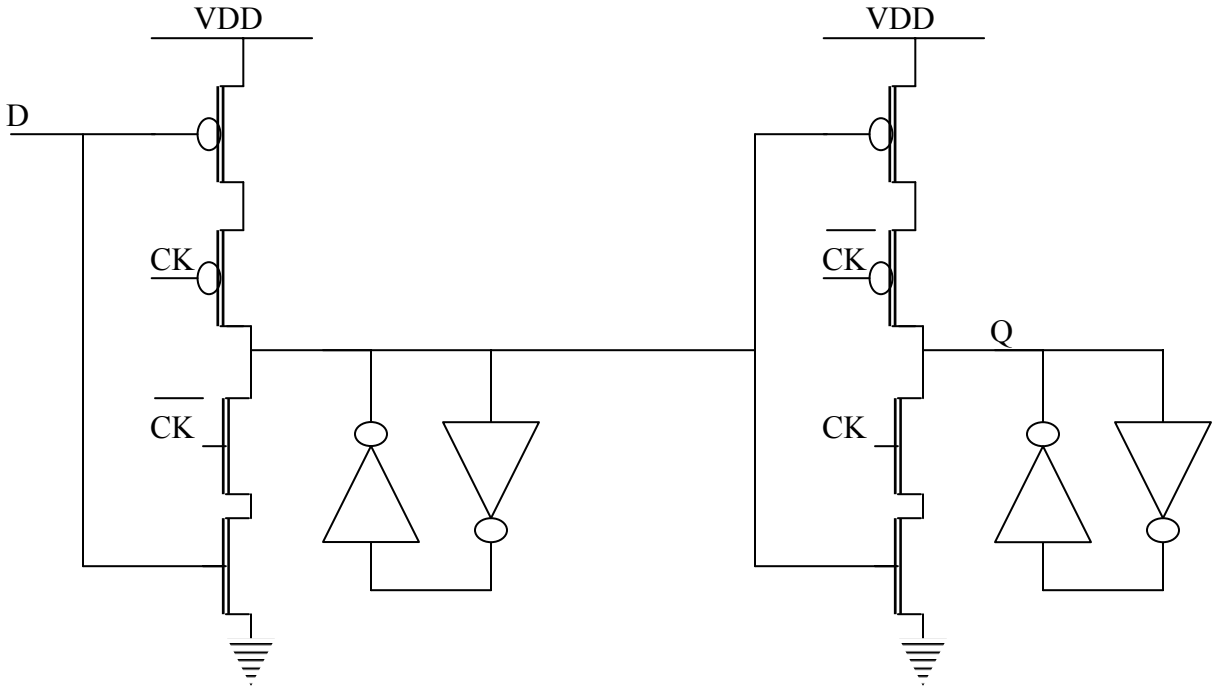
A Bus: A connection with multiple Drivers and Receivers



It can be used as a latch:



A MASTER-SLAVE FF (Positive edge triggered)



For Negative edge triggered➔ exchange the positions of CK and $\overline{CK}$

True-Single-Phase-Clock(TSPC) FF:

All FFs seen so far need both CK and $\overline{CK}$ (2 phase clocks)