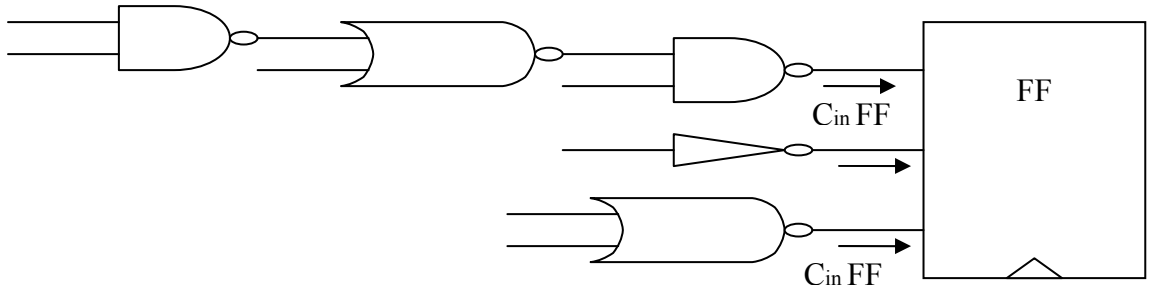
Synchronous Circuit Design, *Continued*

4- Design all logic in between FFs starting with the last level where $C_L = C_{in}$ of the FF:

Then we proceed to the next logic level where its load is C_{in} of the last logic level pulse any wiring capacitance…continued till we design the first logic level.



If the C_{in} of the first level is greater than the value we assumed as load for the FF then the circuit can not be designed to meet the required clock frequency ((either re-do the logic design to reduce the number of the logic levels, or do architectures changes such as pipelining to reduce to reduce the number of logic levels in between FFs.

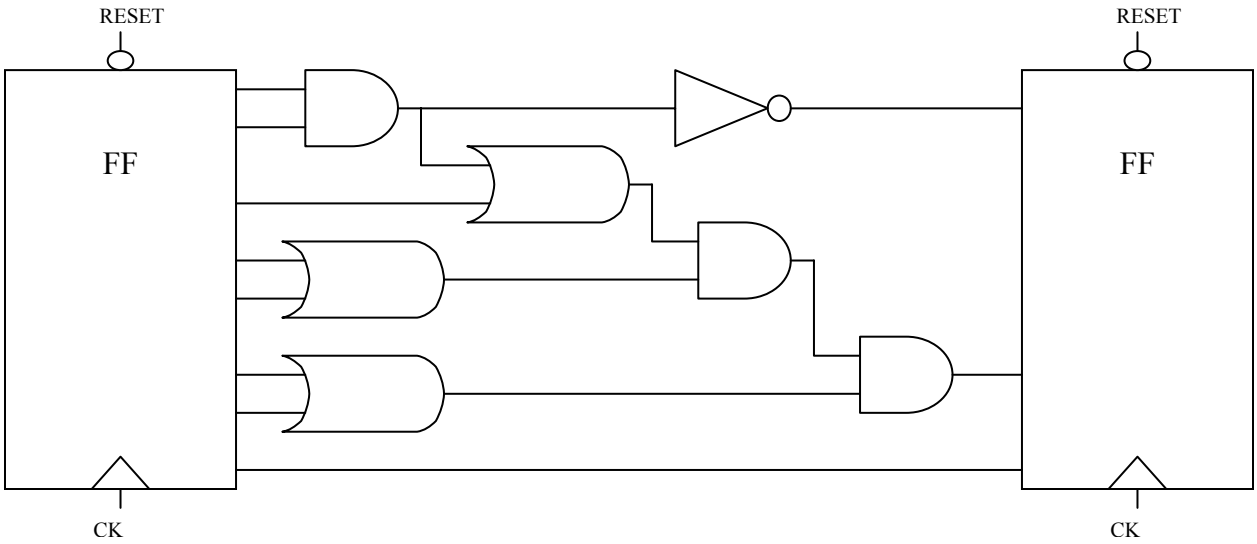
- The general formula for calculating C_L for any Gate:

$C_L = \sum C_{in} + \sum C_{wire}$

Sum of all input capacitances of gates connected to the output + sum of all wires capacitance connected to the output.

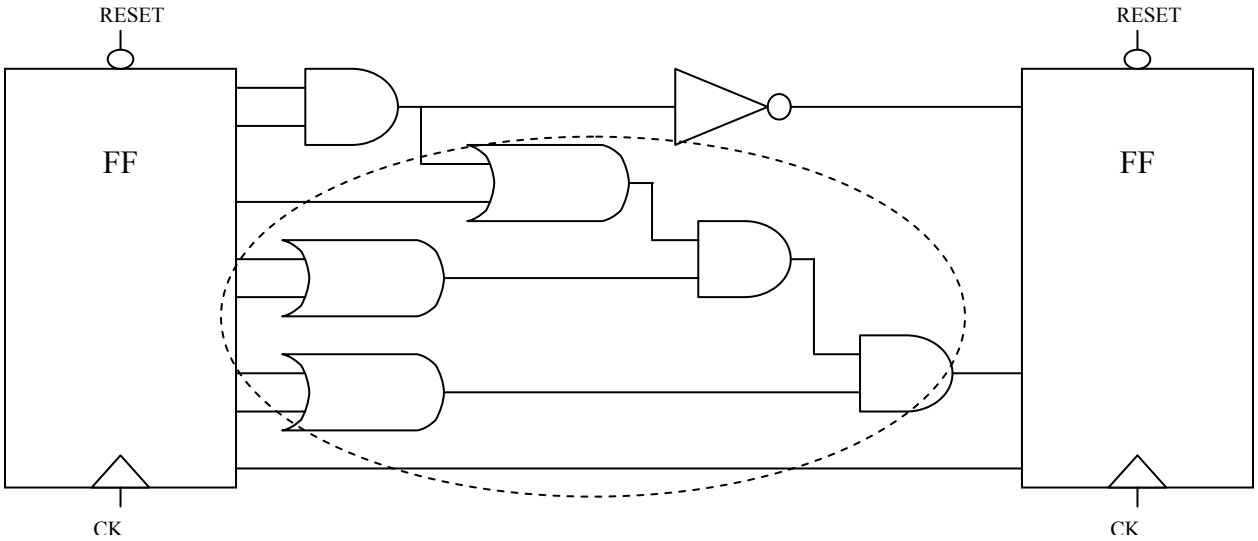
- Try to re-use gates if C_L of the second gate is less than or equal to C_L of the already designed gate and the required delay is bigger than or equal to that of the designed gate.

Example:
Design the following circuit in CMOS to operate at 2GHz. Use the 1_{um} technology and assume that $T_{skew} = 50_{ps}$ and $T_{jitter} = 20_{ps}$.

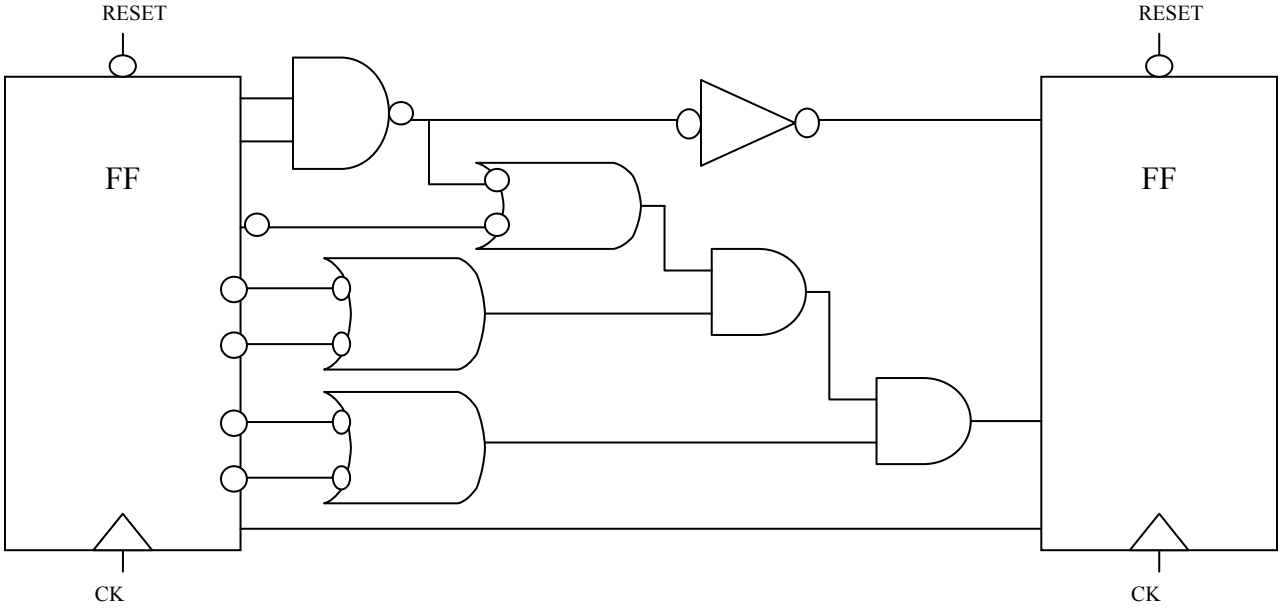


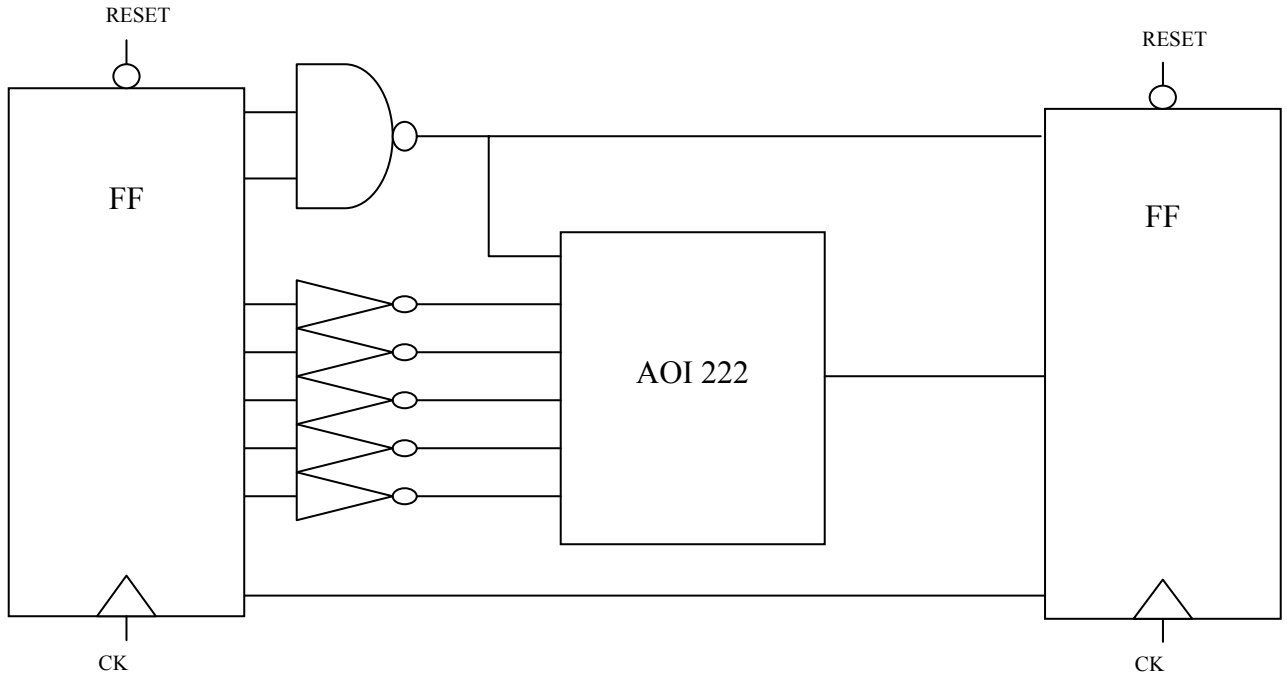
Sol:

Try to combine groups (or clusters) of gates into single gates:



Then convert to CMOS (insert bubbles):

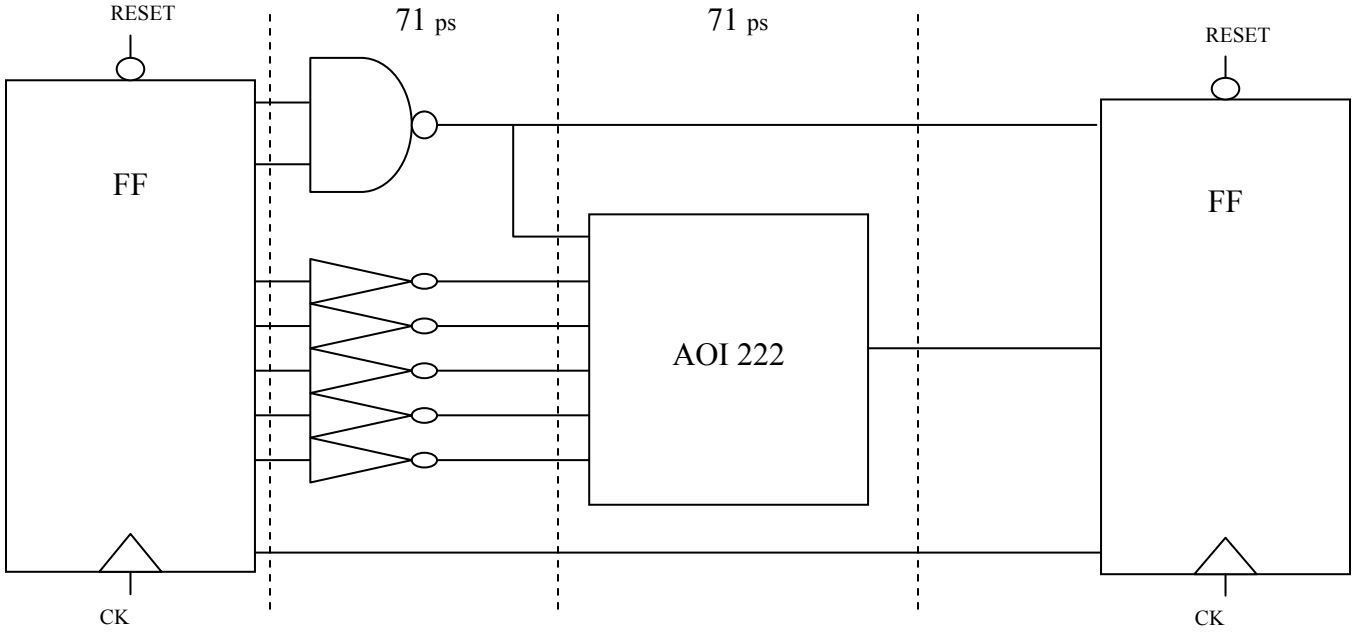




Total number of logic levels, including the FF = 2 + 4 = 6
T_{CK} = 1/2GHz = 500 ps

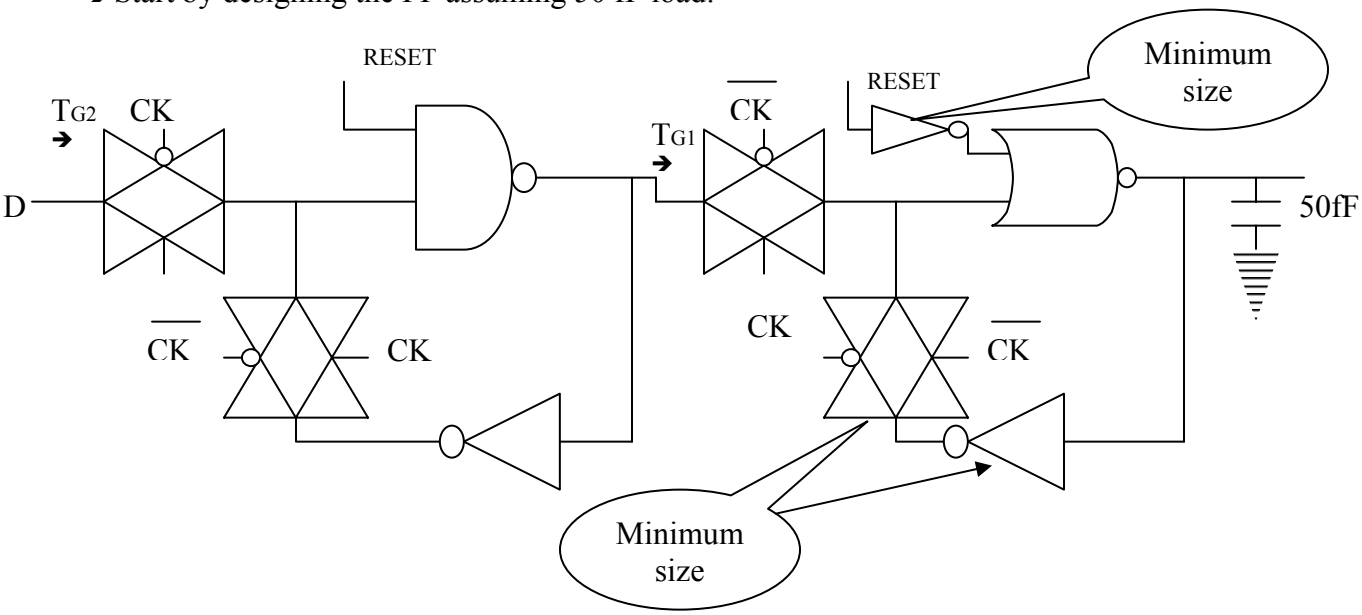
Delay per logic level = $\frac{T_{CK} - T_{skew} - T_{jitter}}{\text{total number of logic}}$

= (500 – 50 – 20) / 6 ≈71 ps



Required T_{SU2} = 2 X 71 = 142 ps and required $T_{CK \rightarrow q1}$ = 2 X 71 = 142 ps

➔Start by designing the FF assuming 50 fF load:



SLAVE logic

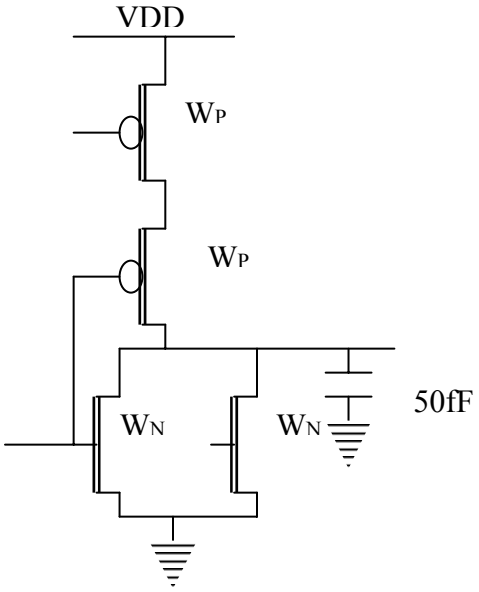
T_D = 71 ps

$W_{Peff} = 2\ W_{Neff}$

$W_{Neff} = W_N$

$W_{Peff} = W_p/2$

➔ $W_P = 4\ W_N$



$R_N = T_D / C_L = 71ps/50fF = 1.4\ K\Omega = (VDD - V_{tn})/ (2I_{Dsat/um} * W_{Neff})$

$W_{Neff} = 4.2/(2X500X10^{6}X1.4X10^{3}) = 2.8$ um $= W_N$

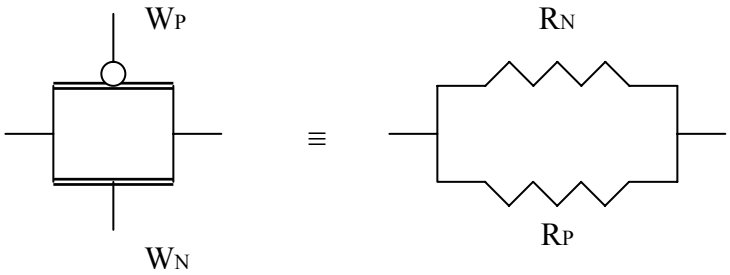
$W_P = 4\ W_N = 11.2$ um

C_{in} = 2fF X1 (2.8 + 11.2) = 28fF

This is C_L for T_{G1}:

To design T_{G1}: Let $W_P = 2\ W_N$

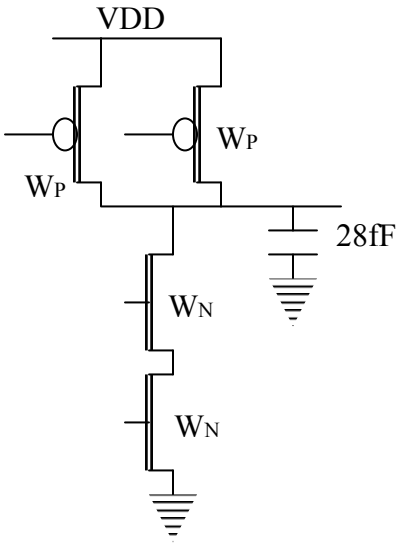
➔ $R_N = R_P$ ➔ $T_D = (R_N /2) * C_L$



➔ $R_N = 2X71 / 28fF \approx 5K\Omega$

➔ $W_N = 4.2/(1000X10^{-6} X5X10^3) \approx 0.8$ um ➔let $W_N = 1$ um and $W_P = 2$ um

Then the MASTER logic



$W_{Neff} = W_N / 2$ $W_{Peff} = W_P$

Let $W_{Neff} = W_{Peff}$ ➔ $W_P = W_N$

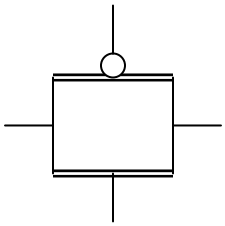
$R_N = T_D / C_L = 71ps / 28fF = 2.5K\Omega$

➔ $W_{Neff} = 4.2 / (1000X10^{-6} X2.5X10^3) \approx 1.6$ um

➔ $W_N = 2X1.6 = 3.2 = W_P$

$C_{in} = 2fF \text{ X } 1\ (3.2+3.2) = 12.8fF$ ➔

This is also C_{in} of the FF



$W_P = 2W_N$

$$R_N = \frac{2T_D}{C_{in} \text{ of the MASTER logic}} = 142ps / 12.8fF \approx 11K\Omega$$

$W_N = 4.2 / (1000X10^{-6} X11X\ 10^3) = 0.4$ um

➔ Let $W_N = 1$ um and $W_P = 2$ um

FF is Done, We do the logic next